A Low-Power 20-GHz 52-dBΩ Transimpedance Amplifier in 80-nm CMOS

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***Abstract*—This paper describes the design of a transimpedance amplifier (TIA) for a low-power, short-distance, high-density fiber-optic interconnect communication system. The single-ended circuit has been designed in an 80-nm digital CMOS process and consumes only 2.2 mW from a 1-V supply. The measured results show a transimpedance gain of 52 dBΩ and a large bandwidth of 20 GHz. This work presents the highest bandwidth at the lowest power consumption for CMOS transimpedance amplifiers reported to date.**

***Index Terms*—CMOS analog integrated circuits, high-frequency CMOS circuits, optical receivers, transimpedance amplifier.**

I. Introduction

THE growth in Internet data traffic and computation power in recent years has increased the demand for more bandwidth in almost all communication systems. Traditionally, the high-speed components in computers or Internet routers are linked by some sort of short-distance electrical medium, such as a printed-circuit transmission line, a twisted pair, or a coaxial cable. Electrical transmission media are severely bandwidth-length limited due to dielectric losses and skin effects. To circumvent this problem, equalization techniques may be employed or more parallel links added. In both cases, this increases the implementation complexity as well as the system cost significantly, whereas the link capacity increases only insignificantly.

A more efficient way to increase the capacity of a short-distance link system is to use inexpensive optical technology. Such an optical link would consist of a low-cost vertical-cavity surface-emitting laser (VCSEL) on the transmitter side, a multimode fiber as transmission medium, and a photodiode on the receiver side. The electrical-to-optical conversion in the VCSEL and the optical-to-electrical conversion in the photodiode impose a significant power loss on the link budget.

However, standard multimode fibers have an attenuation in the range of 3–5 dB/km at an optical wavelength of 850 nm and, therefore, feature significantly lower loss than electrical transmission media do. Multimode fibers are limited by their bandwidth-length products, which typically are on the order of 150–400 MHz · km.

One of the most critical building blocks in an optical link system is the transimpedance amplifier (TIA), which converts the photodiode (PD) current into an amplified voltage. The requirements for a typical TIA are high bandwidth, high transimpedance gain, adequate power gain, low noise, low input impedance, small area, and low power consumption for array applications.

The major design goals of this work were a high bandwidth and minimal power consumption. For short-distance links, higher input-referred noise currents can be tolerated than for long-distance links.

Until now, TIAs with a bandwidth greater than 10 GHz could only be built in GaAs, InP, or SiGe technology. Table I shows a comparison of recently published TIAs. The minimum gate length has been included for designs in CMOS technology.

TABLE I
COMPARISON OF HIGH-SPEED TRANSIMPEDANCE AMPLIFIERS

BW [GHz]	Technology	R [Ω]	P [mW]	Input-ref. Noise [pA/√Hz]	Ref.
8.3	HEMT	700	-	8.8	[1]
8.0	HEMT	1460	500	6.5	[2]
9.0	BiCMOS	560	140	11.5	[3]
1.2	GaAs	1625	120	6.1	[4]
49	InP HEMT	400	-	-	[5]
1.0	0.7-µm CMOS	1000	100	7	[6]
1.25	0.35-µm CMOS	1500	40	16	[7]
0.55	0.6-µm CMOS	8700	30	4.5	[8]
1.2	0.5-µm CMOS	800	115	17.3	[9]
2.6	0.18-µm CMOS	861	47	13	[10]
3.5	0.6-µm CMOS	1122	135	4.2	[11]
19	80-nm CMOS	178	6.5	-	[12]
20	**80-nm CMOS**	**400**	**2.2**	**50**	**This Work**

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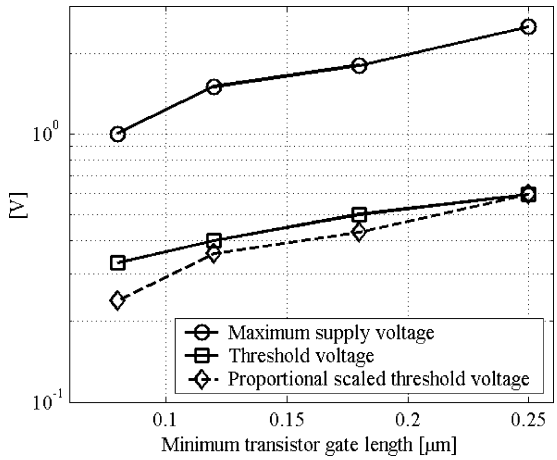

Fig. 1. Maximum supply voltage and threshold voltage versus minimum transistor gate length of a typical downscaled CMOS technology, according to the technology design manuals. The dashed line shows how a proportional threshold voltage scaling would look.

As CMOS technology is downscaled to gate lengths of 80 nm and less, the peak transit frequency of an nMOS transistor is pushed to over 100 GHz [13]. Therefore, the design of circuits in CMOS technology operating at 10 GHz should be straightforward. However, the downscaling of CMOS devices has certain drawbacks that make the design of RF circuits in CMOS challenging.

First, the transit frequency of over 100 GHz is usually measured and extrapolated at a device biased at the maximum supply voltage. This is not practical for analog circuit design. Instead, transistors are biased with no more than half the maximum voltage supply. Therefore, the transit frequency of a transistor at a practical bias is typically 50% lower. The transit frequency versus drain current at different drain–source voltages of a 100-nm CMOS technology is shown in [13].

Second, with the geometric shrinking of the devices, the maximum supply voltage has also been decreased to prevent destructive breakdown in the CMOS transistor and to save power in digital VLSI systems. The threshold voltage has not been lowered proportionally to the maximum supply voltage. Therefore, with fixed supply voltage, transistors cannot be cascaded, nor can the maximum circuit speed be maintained. Fig. 1 shows the downscaling trend of a typical CMOS technology. Third, the drain–source leakage of the transistors will increase considerably if downscaling is applied. As a consequence, the intrinsic voltage gain of a transistor with a channel length of 80 nm is less than 10. Therefore, more than one stage is needed for high-gain RF amplifier circuits, which increases the overall power consumption and may jeopardize the circuit's stability if feedback is employed.

II. Optical-Link Budget

The optical power loss in a short-distance multimode link is mainly caused by electro-optical conversion and fiber coupling. Electro-optical conversion typically takes place in the VCSEL and the photodiode. A typical VCSEL emits 2 mW of optical power [14]. The total coupling loss is on the order of 3 dB. For short-distance links, multimode fiber attenuation can be neglected. This results in a typical optical power $P_{\text{in}}^{\text{opt}}$ of 0 dBm, incident to the active area of the photodiode.

A simple system analysis that considers only bit errors due to device noise results in the following expression for photoreceiver sensitivity:

$$P_{\text{in,min}}^{\text{opt}} = \frac{\text{SNR}}{2 \cdot \Re} \sqrt{\overline{I_{\text{ni}}^2} \cdot \Delta f} \tag{1}$$

where $P_{\text{in,min}}^{\text{opt}}$ is the minimum optical power averaged over the time necessary to achieve a given SNR for nonreturn-to-zero (NRZ) data. SNR stands for the required signal-to-noise ratio for a certain bit-error rate (BER). The required SNR for a BER of 10^{-12} is 14 dB [17] for NRZ signaling, matched filter detection, and in the presence of additive white Gaussian noise (AWGN). $\Re$ denotes the photodetector responsivity. Typical values for the responsivity of p-i-n photodiodes are in the range of 0.4–0.6 A/W at an optical wavelength of 850 nm. The parameter Δf stands for the receiver's effective bandwidth, over which the total input-referred mean-square noise-current spectral density $\overline{I_{\text{ni}}^2}$ of the photodetector and the amplifier noise is integrated:

$$\overline{I_{\text{ni}}^2} = \overline{I_{PD}^2} + \overline{I_{\text{ni,amp}}^2}. \tag{2}$$

The predominant noise source in p-i-n photodiodes is shot noise, which can be expressed as a mean-square noise-current spectral density in the following form:

$$\overline{I_{PD}^2} = \overline{I_{shot}^2} = 2qI_D \tag{3}$$

where q denotes the electron charge and I_D the photodiode current. The noise sources in a broadband CMOS TIA are the thermal channel and induced gate noise.

For short-distance optical-interconnect applications, the photodiode will operate at high current levels, e.g., 0.5 mA, if $P_{\text{in}}^{\text{opt}} = 0$ dBm and $\Re = 0.5$ A/W. Using (3), a root mean square (rms) shot-noise current spectral density of 13 pA/$\sqrt{\text{Hz}}$ is obtained. This can be defined as an upper design limit for the allowed amplifier noise. Assuming that the photodiode and amplifier contribute an rms current spectral density of 13 pA/$\sqrt{\text{Hz}}$, a BER of 10^{-12}, and a bandwidth of 20 GHz, (1) yields a sensitivity of -11.8 dBm. The receiver sensitivity requirement is relaxed somewhat because multimode-fiber attenuation can be neglected. However, power consumption has to be minimized, and the bandwidth should be maximized.

III. Classical Resistive-Shunt Feedback TIA

Various TIA topologies in CMOS have been studied extensively in the past [7]. All circuit topologies that include a cascode or a source follower are not considered further here because, as mentioned in Section I, deep-submicron CMOS technology does not allow two gate–source voltages to be stacked and maximum circuit speed to be maintained at a low power supply.

Fig. 2 shows the schematic of a conventional single-stage resistive shunt feedback TIA in common-source configuration.

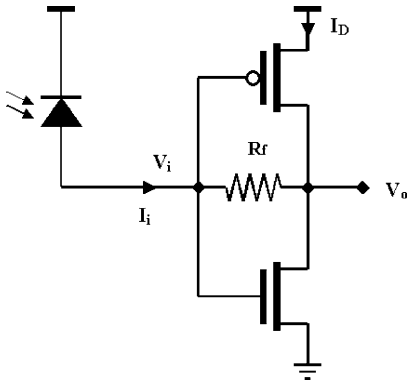

Fig. 2. Schematic of a single-stage resistive shunt feedback CMOS TIA in common-source configuration with a photodetector.

The dc transimpedance gain Z_{TIA} and the input impedance Z_i can be calculated as follows:

$$Z_{\mathrm{TIA}} = \frac{V_o}{I_i} = \frac{g_m - g_f}{g_f\,(g_m + g_{ds})} \tag{4}$$

$$Z_i = \frac{V_i}{I_i} = \frac{g_{ds} + g_f}{g_f\,(g_m + g_{ds})} \tag{5}$$

where $g_f = 1/R_f$, $g_m = \alpha \cdot I_d$, and $g_{ds} = g_m/A_o$. The parameter A_o is the intrinsic gain of the transistors and has a value of roughly 8. The parameter α reaches approximately 13 V^{-1} at the bias point in this 80-nm CMOS technology. The parameter R_f denotes the feedback resistance and I_d the drain current. Finally, g_m is the total nMOS and pMOS small-signal transconductance, and g_{ds} the total nMOS and pMOS transistor output conductance at the bias point.

The light-sensitive area of an 850-nm p-i-n photodiode for 10-Gb/s applications typically has a diameter of 60 μm. The depletion capacitance C_{dep} is the predominant capacitance in the system and, together with the input pad capacitance C_{pad} of the TIA, it forms the dominant pole in the frequency response.

For a given total input capacitance of $C_{\mathrm{i,tot}} = C_{\mathrm{dep}} + C_{\mathrm{pad}}$ and a required bandwidth of $f_{-3\mathrm{dB}}$, the input impedance is determined by

$$Z_i = \frac{1}{2\pi f_{-3\mathrm{dB}} \cdot C_{\mathrm{i,tot}}}. \tag{6}$$

From (4)–(6), the required feedback resistance R_f and the transimpedance gain Z_{TIA} for the circuit in Fig. 2 can be calculated. The results are plotted in Fig. 3.

Fig. 3 clearly shows that, with this circuit topology in 80-nm CMOS, a transimpedance gain of over 200 Ω can only be achieved by supplying a current of at least 100 mA in a single-ended configuration. This is not a practical solution for a high-density link application, where hundreds of links are placed on one chip and the power budget per link is on the order of 20–30 mW/(Gb/s). One link contains a transmitter and a receiver with clock-and-data recovery (CDR). The high-impedance output of the amplifier would have to be decoupled from the feedback resistor R_f by means of a source-follower stage. The source-follower stage requires the headroom of another gate–source voltage, which does not allow the amplifier to operate at its maximum bandwidth. Another drawback in the topology of Fig. 2 is the large capacitance associated with the pMOS transistor, which decreases the amplifier bandwidth considerably.

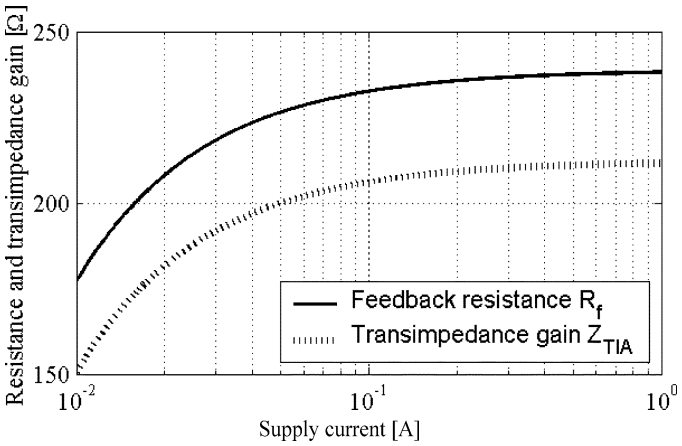

Fig. 3. Feedback resistance and transimpedance gain are computed and displayed versus supply current of the shunt feedback TIA implementation. In this example $C_{\mathrm{i,tot}} = 300$ fF and $f_{-3\mathrm{dB}} = 20$ GHz have been assumed.

In order to build a TIA with the classical resistive-shunt feedback approach, the amplifier requires more than one gain stage, which in turn raises stability concerns.

IV. Common-Gate Feedforward TIA

A. Implementation

A conventional regulated cascode [11], [15] is shown in Fig. 4(a). In this circuit topology, the headroom of two gate–source voltages at the V_y circuit node and one gate–source plus one drain–source saturation voltage at the V_o circuit node are required. Two gate–source voltages exceed the voltage supply limit of 1 V if the transistors are biased at least at half the supply limit. The biasing of the transistors could be decreased to fit into the 1-V supply limit. However, then the speed of the regulated cascode would also be significantly decreased.

The single-ended circuit shown in Fig. 4(b) is a modified conventional regulated cascode. The modification is that transistor M_2 has been inserted, which acts as a pass transistor and shifts the gate voltage of M_3 to a higher level. This circumvents the problem of the conventional regulated cascode, which requires two transistor gate–source voltages at the V_y node. By introducing M_2, all amplifying transistors can be biased at a gate–source and a drain–source voltage equal to or higher than 0.5 V.

The implemented TIA is a common-gate topology with a gain-enhancing feedforward path and an input-impedance reducing feedback. Transistor M_1 provides the feedback; the feedforward path is formed by M_2 and M_3. Transistor M_4 operates as the current source.

B. Transimpedance Gain

A small-signal analysis yields the following equations of the summed currents at the circuit nodes V_i, V_x, V_y, and V_o:

$$\begin{aligned} I_i = {} & V_i\,(g_{m1} + g_{mb1} + g_{ds1} + g_{m2} \\ & + g_{mb2} + g_{ds2} + g_{ds4} + j\omega C_{\mathrm{i,tot}}) \\ & - V_x\,(g_{ds2} + j\omega C_{ds2}) - V_y\,(g_{m1} + j\omega C_{gs1}) \\ & - V_o\,(g_{ds1} + j\omega C_{ds1}) \end{aligned} \tag{7}$$

$$\begin{aligned} 0 = {} & V_x\,(y_2 + g_{ds2} + j\omega\,[C_{d2} + C_{g3}]) - V_y j\omega C_{gd3} \\ & - V_i\,(g_{m2} + g_{mb2} + g_{ds2} + j\omega C_{ds2}) \end{aligned} \tag{8}$$

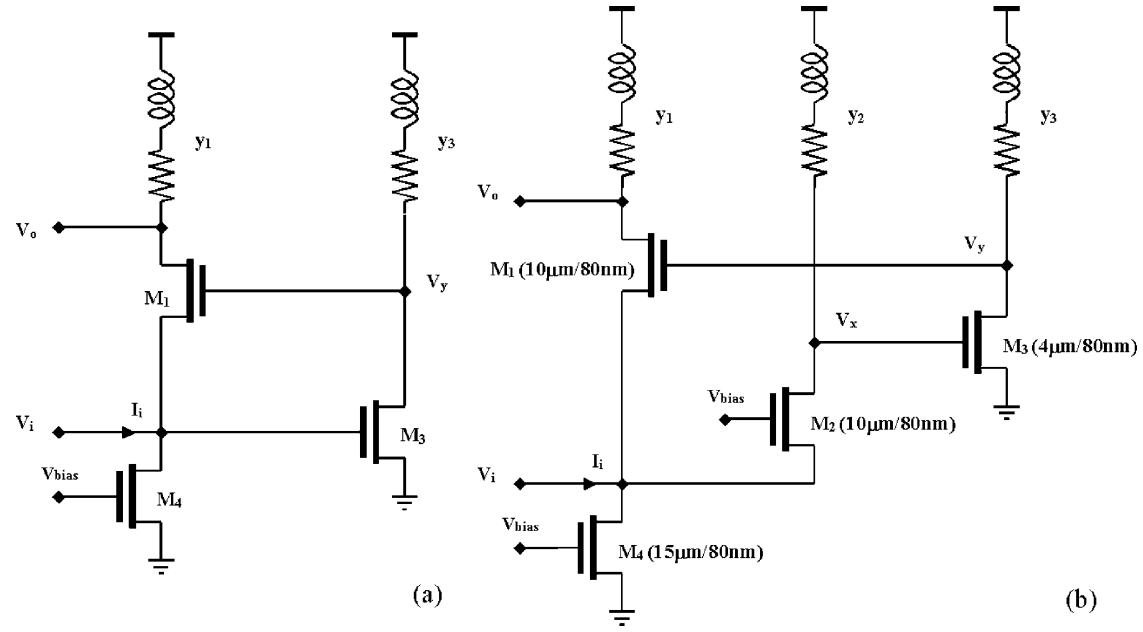

Fig. 4. (a) Schematic of the conventional single-ended regulated cascode. (b) Schematic of the single-ended common-gate feedforward TIA designed. Next to the transistor references, the gate widths and lengths are indicated in parentheses.

$$0 = V_y\left(y_3 + g_{ds3} + j\omega\left[C_{d3} + C_{g1}\right]\right) - V_x\left(g_{m3} - j\omega C_{gd3}\right) - V_o j\omega C_{gd1} - V_i j\omega C_{gs1} \tag{9}$$

$$0 = V_o\left(y_1 + g_{ds1} + j\omega\left[C_{d1} + C_L\right]\right) + V_y\left(g_{m1} - j\omega C_{gd1}\right) - V_i\left(g_{m1} + g_{mb1} + g_{ds1} + j\omega C_{ds1}\right) \tag{10}$$

where g_{mx} is the gate–source transconductance, g_{mbx} the bulk–source transconductance, g_{dsx} the output conductance or leakage, C_{dx} the total drain capacitance, C_{gx} the total gate capacitance, C_{dsx} the drain–source capacitance, C_{gdx} the gate–drain capacitance, and C_{gsx} the gate–source capacitance of the transistor M_x. The parameter y_x denotes the load admittance connected to the transistor M_x and consists of an integrated resistor in series with a spiral inductor. The total input capacitance is $C_{\mathrm{i,tot}} = C_{d4} + C_{s1} + C_{s2} + C_{\mathrm{pad}} + C_{\mathrm{dep}}$, where C_{sx} represents the total source capacitance of transistor M_x, C_{pad} the input pad capacitance, and C_{dep} the photodiode depletion capacitance. C_L denotes the capacitive load of the stage following the TIA.

For simplicity, g_{mbx} and g_{dsx} can be neglected because $g_{mx} \gg g_{mbx}$, $y_x \gg g_{dsx}$ and $g_{mx} \gg g_{dsx}$. The existence of more than one path between the input and the output node usually creates a zero in the transfer response. The drain–source and gate–drain capacitances C_{ds1}, C_{ds2}, C_{gd1}, and C_{gd3} introduce parasitic zeros at $\omega_{z,ds1} \approx g_{m1}/C_{ds1}$, $\omega_{z,ds2} \approx g_{m2}/C_{ds2}$, $\omega_{z,gd1} \approx g_{m1}/C_{gd1}$, and $\omega_{z,gd3} \approx g_{m3}/C_{gd3}$, respectively. The frequencies of these zeroes are a factor of >10 higher than the TIA bandwidth of interest. Therefore, the parasitic capacitances C_{ds1}, C_{ds2}, C_{gd1}, and C_{gd3} can be neglected as well.

By applying the simplifications discussed above, the small-signal equations (8) and (9) yield the following gains of transistors M_2 and M_3:

$$A_2 = \frac{V_x}{V_i} \approx \frac{g_{m2}}{y_2 + j\omega\left[C_{d2} + C_{g3}\right]} \tag{11}$$

$$A_3 = \frac{V_y}{V_x} \approx -\frac{g_{m3}}{y_3 + j\omega\left[C_{d3} + C_{g1}\right]}. \tag{12}$$

From (10)–(12), the total voltage gain of the circuit is

$$A = \frac{V_o}{V_i} \approx \frac{g_{m1}\left(1 - A_2A_3\right) + g_{mb1} + g_{ds1}}{y_1 + g_{ds1} + j\omega\left[C_{d1} + C_L\right]}. \tag{13}$$

Equation (13) can be simplified to

$$A = \frac{V_o}{V_i} \approx A_1\left(1 + |A_2A_3|\right). \tag{14}$$

The gain of transistor M_1 is approximately

$$A_1 \approx \frac{g_{m1}}{y_1 + j\omega\left[C_{d1} + C_L\right]}. \tag{15}$$

The small-signal voltage gain A is calculated using (14) and (15), and the result is shown in Fig. 5. The small-signal parameters are obtained from SPICE simulations.

From (7), (11), and (12) and by applying the simplifications above, the input impedance of the circuit can be expressed as follows:

$$Z_i = \frac{V_i}{I_i} \approx \frac{1}{g_{m1}\left(1 - A_2A_3\right) + g_{m2} + g_{ds4} + j\omega\left[C_{\mathrm{i,tot}} + A_2A_3C_{gs1}\right]} \tag{16}$$

which, by assuming $g_{m2} + g_{ds4} \ll g_{m1}\left(1 - A_2A_3\right)$ and $A_2A_3C_{gs1} \ll C_{\mathrm{i,tot}}$, can be reduced to

$$Z_i \approx \frac{1}{g_{m1}\left(1 + |A_2A_3|\right) + j\omega C_{\mathrm{i,tot}}} \tag{17}$$

which is displayed in Fig. 6.

The transconductance g_{m1} is increased by a factor of $1 + |A_2A_3|$, which allows M_1 to be reduced and subsequently M_2 and M_3 by the same amount, while keeping Z_i constant. Thus,

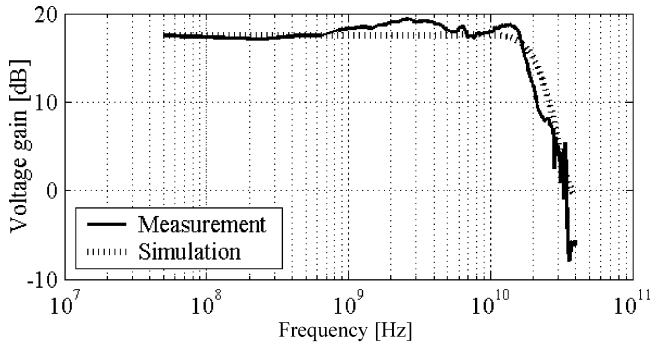

Fig. 5. Comparison of the measured and simulated voltage gain of the TIA design.

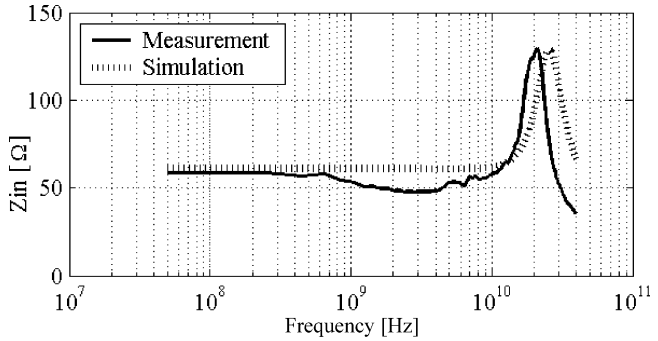

Fig. 6. Simulated and measured input impedance of the common-gate feedforward TIA design.

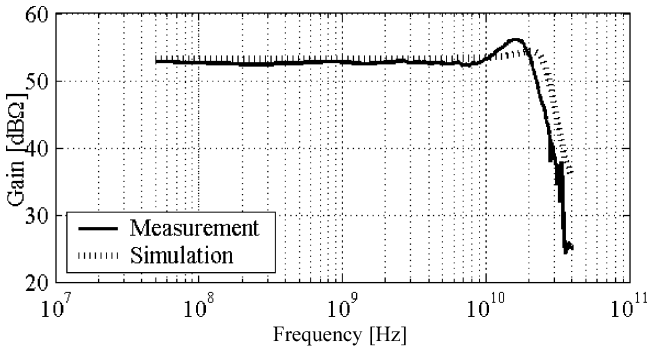

Fig. 7. Transimpedance gain measurement and simulation of the common-gate feedforward TIA design.

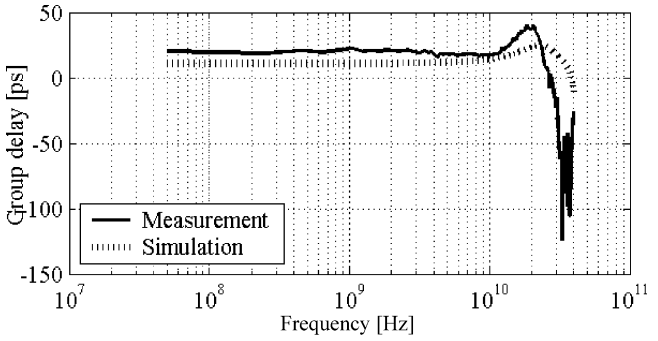

Fig. 8. Transimpedance group delay measurement and simulation of the TIA design. The measurement shows a maximum group delay ripple of ±20 ps up to 25 GHz.

the power consumption can be significantly reduced by a factor of $(1+|A_2A_3|)/3$, compared to a single-stage common-gate implementation. It is assumed that M_1, M_2, and M_3 draw the same amount of current. In comparison, the power assumption of a conventional regulated cascode can be reduced by a factor of only $(1+|A_3|)/2$.

In addition, the input impedance faces capacitive peaking because the frequency of the dominant pole of $|A_2A_3|$ is lower than that of the dominant pole

$$\omega_{Zi} = \frac{g_{m1}+g_{m2}}{C_{s,tot}} \tag{18}$$

of the input impedance.

The transimpedance gain Z_{TIA} can be derived from (14) and (17) as follows:

$$Z_{\mathrm{TIA}} = \frac{V_o}{I_i} = Z_i A = \frac{1}{y_1 + j\omega\left[C_{d1}+C_L\right] + \frac{j\omega C_{\mathrm{i,tot}}}{A}}. \tag{19}$$

By assuming $C_{d1}+C_L \ll C_{\mathrm{i,tot}}/A$, the result in (19) reduces to

$$Z_{\mathrm{TIA}} = \frac{1}{y_1 + \frac{j\omega C_{\mathrm{i,tot}}}{A}}. \tag{20}$$

Figs. 7 and 8 show the calculated transimpedance gain and the group delay of (20).

The capacitive peaking of Z_i increases the bandwidth of the transimpedance gain. For sufficiently low frequencies, the transimpedance gain can be approximated by

$$Z_{\mathrm{TIA}} \approx \frac{1}{\mathrm{Re}\,(y_1)}. \tag{21}$$

Owing to process variation, g_m and g_{ds} and therefore A_1, A_2 and A_3 may vary considerably. However, for sufficiently low frequencies, the TIA gain depends mainly on the real part of the load admittance y_1, which is an integrated salicided polyresistor in series with the sheet resistance of the spiral inductor. The polyresistor can be manufactured within the moderate process variations of $\pm 20\%$ in this case.

The degrees of freedom for the design of this TIA are limited. Similarly, as seen in the example of the shunt-feedback TIA in Section III, the input impedance is predetermined for a desired bandwidth and a given photoreceiver capacitance. The gain factor $1+|A_2\cdot A_3|$ is maximized while its bandwidth is kept well above the bandwidth of the desired voltage gain A. According to (17), g_{m1} and therefore the size of M_1 are determined.

C. Gain-Bandwidth-Enhancing Features

In (11)–(19), we observe a number of gain-enhancing features of this topology. First, from (14), we can derive that by choosing $|A_2\cdot A_3| \geq 1$ and the frequency of the dominant pole of $A_2\cdot A_3$ to be sufficiently above the frequency of the dominant pole of A_1, the total gain will be at least doubled and

the bandwidth will remain close to that of A_1. We know that if we cascade two equivalent common-source amplifiers, their gains get multiplied, but the bandwidth of the resulting circuit is reduced by 35%. Second, as the input signal is injected at the sources of transistors M_1 and M_2, their substrate conductances further help to increase the gain [see (8) and (13)]. Third, at each high-impedance circuit node V_x, V_y, and V_o, the transistors drive their total drain capacitance plus only one total gate capacitance as a load. This strategy helps to minimize the total capacitive load at each high-impedance circuit node and therefore increases the overall circuit bandwidth.

Peaking inductors further help to increase the bandwidth of the TIA [9]. The peaking inductors do not require a high Q factor, and can thus be optimized for low parasitic capacitances and small area. Large spiral inductors tend to consume a large chip area. Therefore, long metal traces may have to be used to connect the RF signals of different circuit blocks, which increases the capacitive load at those nodes and consequently may decrease the speed of the circuit.

The spiral inductors use the top two metal layers of a 6-metal layer process in series. A minimal trace width has been chosen such that it just fulfills the electromigration rules with a margin. The minimal interwinding spacing was selected according to layout design rules. Each inductor has eight turns and occupies a chip area of only 18 μm $\times$ 18 μm. The inductors are very compact, allowing the total chip area to be minimized.

The peaking inductors have been implemented separately on a test structure in order to verify the field-solver simulation. Measurements of the inductor reveal a series inductance of 2.2 nH and a series resistance of 75 Ω versus a simulated inductance of 2.7 nH and a simulated series resistance of 73 Ω by the field solver. That the measured inductance is lower than the simulated one is believed to be caused by the mandatory minimum metal filling, which can be seen in the spiral inductor portion of Fig. 13.

D. Noise Analysis

When CMOS transistors operate at radio frequencies, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate-oxide capacitance and cause the induced gate noise, which is usually correlated with the channel noise. The van der Ziel [18] model shown in Fig. 9 is well accepted and has a physical basis:

$$\overline{I_d^2} = \widehat{I_d}^2 = 4kT\alpha g_m \tag{22}$$

$$\overline{I_g^2} = \widehat{I_g}^2 = 4kT\delta g_g \tag{23}$$

where $\alpha = \gamma g_{d0}/g_m$, γ is he coefficient of the channel thermal noise, k the Boltzmann constant, T the absolute temperature, δ the coefficient of the gate noise, $\overline{I_d^2}$ the mean-square channel, and $\overline{I_g^2}$ the induced gate-noise current spectral density. $\widehat{I_d}$ and $\widehat{I_g}$ represent the rms channel and induced gate-noise current spectral densities, respectively. The shunt conductance g_g is

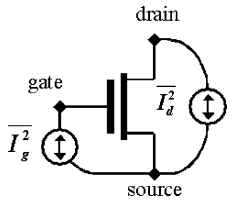

Fig. 9. Van der Ziel thermal-noise model of a MOSFET.

$$g_g = \frac{\omega^2 C_0^2}{g_{d0}} \tag{24}$$

where g_{d0} is the zero-bias drain conductance and C_0 the gate-oxide capacitance of the MOS transistor. The correlation term is given by

$$\overline{I_d I_g^*} = c\sqrt{\overline{I_d^2} \cdot \overline{I_g^2}} \tag{25}$$

where c is the cross-correlation coefficient between the drain and gate noise. For long-channel MOS nFETs, values for γ, δ, and c are 2/3, 16/135, and $j0.395$, respectively, and $g_{d0} = g_m$. Short-channel effects increase γ and δ. Furthermore $g_{d0} \geq g_m$ [18].

The noise calculation for the implemented circuit is nontrivial. If a MOSFET is used in common-gate configuration, the source of the transistor becomes a signal node. Therefore, the channel noise power, which is injected at the drain and at the source, is fully correlated. The correlation coefficient is -1. The same applies to the induced gate noise power at the gate and at the source, where the correlation coefficient is 1.

To evaluate the noise performance of the TIA efficiently, the following method is proposed. First, all mean-square noise-current spectral densities of all noisy circuit elements at each circuit node are referred to the output of the circuit. Second, the mean-square noise voltage spectral densities are added at the output. The amplitudes of the correlated portion of the noise spectral densities must be summed before the powers of the various contributors are summed. Third, the total noise power spectral density at the output is referred to the input.

The mean-square channel thermal-noise voltage spectral density generated by M_1, M_2, and M_3 can be calculated as follows:

$$\overline{V_{no,d1}^2} = \left(\widehat{I_{d1}} Z_i A - \widehat{I_{d1}} Z_o\right)^2 = 4kT\alpha g_{m1}(Z_{\mathrm{TIA}} - Z_o)^2 \tag{26}$$

$$\begin{aligned}\overline{V_{no,d2}^2} &= \left(\widehat{I_{d2}} Z_i A - \widehat{I_{d2}} Z_x A_{xo}\right)^2 \\ &= 4kT\alpha g_{m2}\,(Z_{\mathrm{TIA}} - Z_x A_{xo})^2\end{aligned} \tag{27}$$

$$\overline{V_{no,d3}^2} = \left(\widehat{I_{d3}} Z_y A_{yo}\right)^2 = 4kT\alpha g_{m3}\,(Z_y A_{yo})^2 \tag{28}$$

where Z_x, Z_y and Z_o are the output impedances at the circuit nodes V_x, V_y and V_o, respectively. Note that the output impedances are not simply the inverse of the load admittances y_1, y_2 and y_3; in fact, feedback reduces Z_x and Z_y to less than half of their values. The parameter A_{xo} stands for the voltage gain from V_x to V_o, and A_{yo} for the voltage gain from V_y to V_o.

The mean-square-induced gate-noise voltage spectral density generated by M_1, M_2, and M_3 is

$$\overline{V_{no,g1}^2} = \left(\widehat{I_{g1}} Z_i A + \widehat{I_{g1}} Z_y A_{yo}\right)^2 = 4kT\delta \frac{\omega^2 C_{01}^2}{g_{d01}} \left(Z_{\mathrm{TIA}} - Z_y A_{yo}\right)^2 \quad (29)$$

$$\overline{V_{no,g2}^2} = \left(\widehat{I_{g2}} Z_i A\right)^2 = 4kT\delta \frac{\omega^2 C_{02}^2}{g_{d02}} \left(Z_{\mathrm{TIA}}\right)^2 \quad (30)$$

$$\overline{V_{no,g3}^2} = \left(\widehat{I_{g3}} Z_x A_{xo}\right)^2 = 4kT\delta \frac{\omega^2 C_{03}^2}{g_{d03}} \left(Z_x A_{xo}\right)^2 \quad (31)$$

where C_{0x} represents the gate-oxide capacitance and g_{d0x} is the zero-bias drain conductance of the transistor M_x. The mean-square channel and the induced gate-noise voltage spectral densities of each transistor M_x can be added as follows:

$$\overline{V_{no,Mx}^2} = \overline{V_{no,dx}^2} + \overline{V_{no,gx}^2} + 2\,|c|\,\sqrt{\overline{V_{no,dx}^2} \cdot \overline{V_{no,gx}^2}}. \quad (32)$$

The noise contribution of the current source M_4 has been accounted for by

$$\overline{V_{no,M4}^2} = 4kT \frac{Z_i^2 A^2}{R_4} = 4kT \frac{Z_{\mathrm{TIA}}^2}{R_4} \quad (33)$$

where R_4 is the equivalent resistance of the current source. The noise contribution of the load resistors and the loss of the peaking inductors can be considered by

$$\overline{V_{no,r}^2} = 4kT \left(\frac{Z_o^2}{R_1} + \frac{Z_x^2}{R_2} A_{xo}^2 + \frac{Z_y^2}{R_3} A_{yo}^2\right) \quad (34)$$

where R_x stands for the resistive part of the load admittances y_x. The total noise at the output of the TIA can be summed as

$$\overline{V_{no}^2} = \overline{V_{no,M1}^2} + \overline{V_{no,M2}^2} + \overline{V_{no,M3}^2} + \overline{V_{no,r}^2}. \quad (35)$$

The total input-referred amplifier mean-square noise-current spectral density can now be derived as

$$\overline{I_{\mathrm{ni,amp}}^2} = \frac{\overline{V_{no}^2}}{Z_{\mathrm{TIA}}^2}. \quad (36)$$

Equations (26)–(31) suggest that the input-referred noise current can be minimized by maximizing A, A_{xo}, and A_{yo} and by minimizing the transconductances and output impedances.

This circuit topology uses relatively small device geometries. The input-referred rms noise-current spectral density is displayed in Fig. 10.

In this design, the TIA has mainly been optimized for gain, bandwidth, and low power consumption. The short-channel values for the noise coefficients γ and δ were not available when the design was done. The noise performance has been found to be sufficient for the target application, assuming a worst case value for $\gamma = 2$ [16].

Fig. 10 shows two sets of rms input-referred noise-current spectral density simulations. For the solid curve, long-channel values for the noise coefficients $\gamma = 2/3$ and $\delta = 16/135$ are assumed. The noise coefficients have higher values in short-channel MOSFETs [8], [18]. The dashed line is computed with noise-coefficient values of $\gamma = 3/4$ and $\delta = 4$.

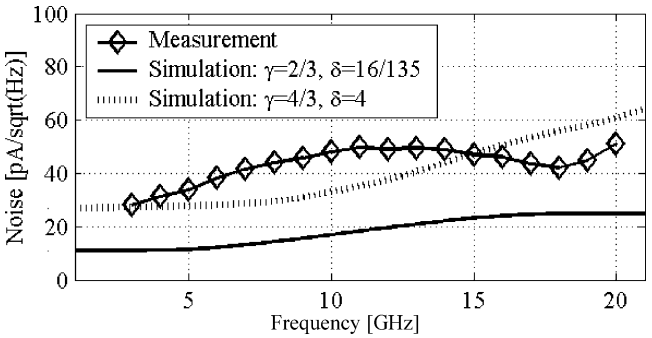

Fig. 10. Measured and simulated input-referred rms noise-current density.

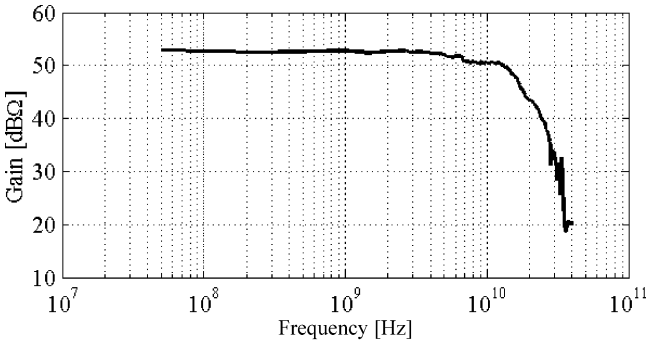

Fig. 11. Transimpedance gain measurement of the common-gate feedforward TIA with a photodiode model included. The depletion capacitance of the photodiode is 220 fF.

V. Measurement Results

The maximum photo current injected into the TIA is 0.5 mA, as mentioned in Section II. Assuming an input impedance of 50 Ω, the maximum signal voltage at the input of the TIA amounts to 25 mVp. Therefore, small-signal analysis is adequate.

In order to evaluate the small-signal performance of the TIA, S-parameters have been measured. The network analyzer input and output power levels have been set to −15 dBm, in order not to saturate the signal. As the stage following the TIA is a limiting amplifier in common-source configuration, the output load of the TIA remains purely capacitive on the order of 5 fF. The large capacitance associated with the output pad needs to be de-embedded. The output pad was implemented separately on a test structure to obtain an accurate de-embeddeding. The input pad is included in the measurement and accommodates approximately 100 fF of parasitic capacitance. From the de-embedded set of S-parameters, the voltage gain, the input impedance, the transimpedance gain, and the group delay can be calculated and are shown in Figs. 5–8, respectively (the photodiode capacitance is not included). The capacitive load of 5 fF has not been included in any of the measurements and simulations. However, this does not significantly change the results because the load capacitance and the output impedance form a pole at 53 GHz. A transimpedance gain measurement, which includes a photodiode model, is shown in Fig. 11. The depletion capacitance in

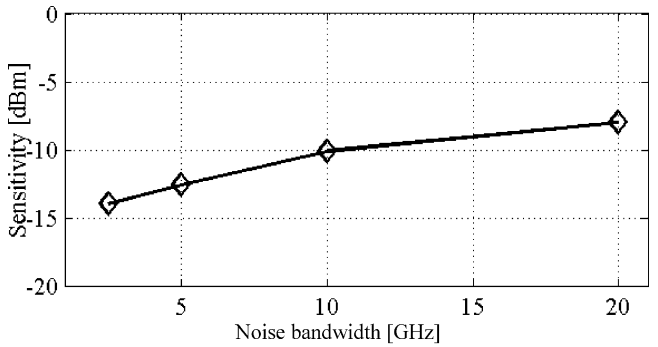

Fig. 12. Data points show the calculated sensitivities for noise bandwidths of 2.5, 5, 10, and 20 GHz. A BER of 10^{-12} and a photodiode responsivity of 0.5 A/W were assumed.

TABLE II
TYPICAL KEY PERFORMANCE PARAMETERS OF THE COMMON-GATE FEEDFORWARD TIA

Performance parameter	Model	Meas.	Units
Transimpedance gain	53.2	52.8	dBΩ
DC input impedance	61	58	Ω
TIA bandwidth without PD	27.2	22.6	GHz
TIA bandwidth with PD	-	13.4	GHz
Power consumption @ 1 V	2.0	2.2	mW
Input-ref. noise @ 3 GHz	27	28	pA/√Hz
Sensitivity @ 20 GHz	-	<–8.0	dBm
Total circuit area	-	0.01	mm²

this case is 220 fF. The input pad capacitance is 100 fF. This results in a total input capacitance of 320 fF. The input pad capacitance could be reduced to approximately 50 fF by optimizing the layout.

The implemented TIA circuit was checked for stability by simulation for all corner cases. The worst case phase margin was 55°. Measurements did not reveal any stability issues.

The transimpedance gain and input impedance measurements are in excellent agreement with the circuit model. The simulations show greater bandwidth, which is believed to be caused by nonmodeled parasitic wiring capacitance.

In order to derive the input-referred noise-current spectral density and subsequently the sensitivity of the TIA, noise parameters have been measured. The input-referred rms noise-current spectral density is less than 50 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for all frequencies up to 20 GHz, as shown in Fig. 10.

The sensitivity of the TIA can be calculated using (1)–(3), whereas the total input-referred amplifier noise $\overline{I_{\mathrm{ni,amp}}^2}$ is shown in Fig. 10. The total input-referred mean-square noise-current spectral density $\overline{I_{\mathrm{ni}}^2}$ is integrated over the desired bandwidth. The sensitivities for noise bandwidths of 2.5, 5, 10, and 20 GHz have been calculated. The results are illustrated in Fig. 12. For a

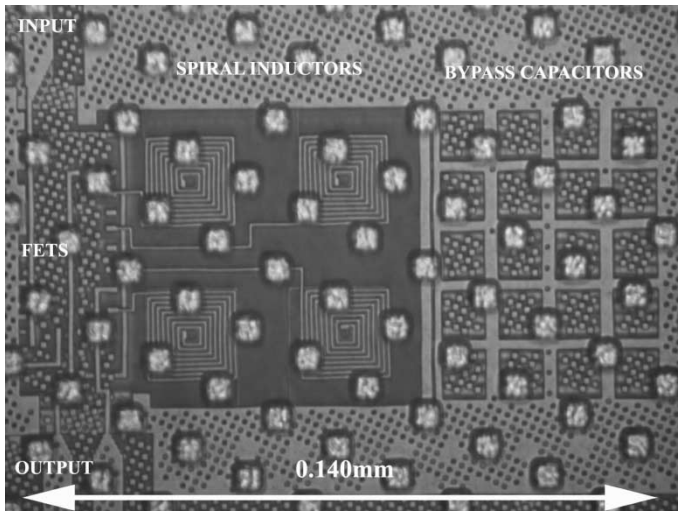

Fig. 13. Photograph of the fabricated circuit.

noise bandwidth of 20 GHz, at least −8.0 dBm optical power incident to the active area of the photodiode is required to achieve a BER of 10^{-12}. A photodiode responsivity of 0.5 A/W was assumed.

As discussed in Section II, in short-distance multimode fiber links, the optical signal power at the photo receiver typically reaches 0 dBm. This leaves a sufficient link margin of 8.0 dB for the largest bandwidth.

The key performance parameters of the single-ended common-gate feedforward TIA are summarized in Table II.

The ripple of the input-referred rms noise-current spectral-density measurement is mainly caused by the peaking of the input impedance, which occurred at a lower frequency in the measurement than predicted by the simulation. The transimpedance bandwidth of the TIA reduces to approximately 20 GHz, assuming a capacitive load of the next stage of about 5 fF.

A photograph of the fabricated circuit is shown in Fig. 13. The circuit occupies a chip area of 140 μm$\times$ 70 μm, and is therefore compatible with the 250-μm pitch typically found in optical receiver arrays.

VI. CONCLUSION

A broadband low-power common-gate feedforward TIA topology for short-distance multimode fiber links in deep-submicron CMOS technology has been implemented and verified. The conventional regulated cascode has been modified for high-speed and low-voltage-supply operation. For short-distance links, the sensitivity may be traded off for a lower power consumption and higher transimpedance bandwidth. The common-gate feedforward TIA topology is well suited to accomplish these requirements. Small signal and noise analyses have been performed. The proposed circuit model shows excellent agreement with measurements. The proposed circuit has been implemented in an 80-nm standard CMOS process. To the knowledge of the authors, the highest transimpedance bandwidth reported to date has been reached for

CMOS transimpedance amplifiers with comparable power consumption.

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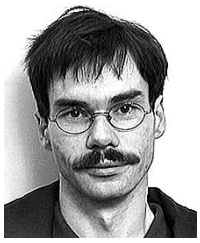

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