A 1-Gb/s, 0.7-μm CMOS Optical Receiver with Full Rail-to-Rail Output Swing

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Abstract—This paper presents a 1-Gb/s optical receiver with full rail-to-rail output swing realized in a standard 0.7-μm CMOS technology. The receiver consists of a 1-kΩ transimpedance preamplifier followed by a postamplifier based on a biased inverter chain. The latter performs both a linear and a limiting amplification. The automatic biasing of the chain is provided through an offset tolerant replica circuit. The receiver requires no external components or biasing voltages. It is designed for a relatively large 0.8-pF input capacitance and is fed from a single 5-V power supply. These properties make the circuit suitable for a commercial environment. A sensitivity of 10 μA was measured at 1 Gb/s. The complete receiver, including all biasing and replicas, consumes approximately 100 mW from the 5-V supply. When powered from a 3.3-V supply, a maximal bit rate of 600 Mb/s is achieved, while the power consumption is reduced to approximately 26.5 mW.

Index Terms—CMOS analog integrated circuits, optical communication, optical receivers.

I. INTRODUCTION

HIGH-SPEED optical communication systems are becoming increasingly important due to the progress of multimedia communication, which requires ever increasing data-transmission capacity. In these systems, there is a strong demand for compact, low-cost receivers. Furthermore, the absence of electromagnetic emission of optical fibers and their inherent insensitivity to electrical interference make them an interesting alternative for high-bit-rate short-to-medium-range electric connections where the shielding costs raise rapidly with the transmission speed and complexity. Interboard or even inter-IC optical connections are, however, only worthwhile when the optical driver and receiver are integrated on the same chip as the digital circuitry that completes the system. Single-chip integration of the optical interface circuit in a cost-effective digital CMOS technology is an answer to both issues.

To be worthwhile in real-life applications, some boundary conditions should be added to the basic optical receiver design. Except for the photodiode, external components and biasing points should be avoided, as they augment the cost and reduce the yield of the system. Furthermore, the foreseen input capacitance must be sufficiently large to allow the use of commercially available photodiodes at the receiver's nominal speed. Single-chip integration is moreover only possible when a rail-to-rail output voltage that may be further processed
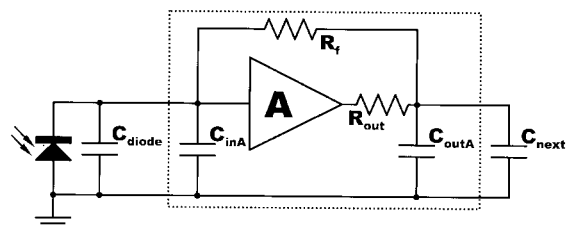
Fig. 1. Generalized schematic of a transimpedance amplifier used in an optical receiver.

digitally is achieved. Last, the receiver must be integrated in a standard digital CMOS process without the use of analog extensions, and it must operate from a single power-supply voltage.

This paper presents a 1-Gb/s optical receiver that fulfills the enumerated requirements. It is realized in a standard 0.7-μm CMOS technology. The receiver consists of two major stages, of which the first is a 1-kΩ transimpedance preamplifier. After a theoretical approach on the optimization of such amplifiers in Section II, the actual circuit is described in Section III. The second stage provides the further amplification to a rail-to-rail output voltage. This postamplifier is based on a biased modified inverter string, as described in Section IV. The accurate biasing of this stage is provided by an offset-tolerant replica biasing circuit. The physical realization of the complete circuit is presented in Section V, while measurement results are given in Section VI.

II. THE TRANSIMPEDANCE AMPLIFIER

The transimpedance amplifier is the most widely used preamplifier structure for high-speed optical receivers (Fig. 1). Its merit is to combine a relatively high transimpedance gain with high speed. For a sufficiently large voltage gain A and small output impedance R_{out}, the closed-loop transimpedance gain of the transimpedance amplifier is given by (1) at the bottom of the next page. The dominant pole is specified by the term in s of the denominator. It can thus be situated either at the input or at the output node. However, as the total input capacitance $C_{\mathrm{in}\,T}$ includes the photodiode capacitance, it is inevitably large compared to the output capacitance $C_{\mathrm{out}\,T}$. This is especially true with an external photodiode, where packaging and interconnection have to be considered. In contrast, the total output capacitance can be limited through a careful layout of both the amplifier and the second stage. In an efficient high-speed design, the dominant pole is therefore located at the input while the output pole is placed sufficiently
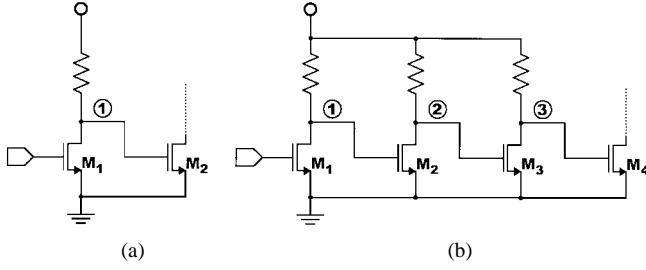
Fig. 2. Simple (a) single-stage and (b) three-stage voltage amplifier.

TABLE I
C_D/C_{GS} FOR SINGLE FINGER TRANSISTORS WITH THE SAME
W/L RATIO IN VARIOUS MODERN CMOS TECHNOLOGIES

	VDB = 0V	VDB = 2.5V	VDB = 5V
.7 µm	1.5	1.0	0.9
.5 µm	1.2	0.8	0.7
.35 µm	1.2	0.7	0.7

high for stability. Equation (1) can then be simplified to

$$Z_{cl} \approx \frac{R_f}{\left(1 + s \cdot \frac{C_{in\,T} \cdot R_f}{A}\right) \cdot (1 + s \cdot C_{out\,T} \cdot R_{out})}. \quad (2)$$

The bandwidth of the transimpedance amplifier is specified by the first pole of its closed-loop transfer function and is given by

$$BW_{Transamp} \approx \frac{1 + A}{R_f \cdot (C_{diode} + C_{in\,A})}. \quad (3)$$

In most communication applications, the transmission speed is a design constraint. The minimal input capacitance is limited by the photodiode, which is determined by technical considerations such as optical rise time, spectral sensitivity, and packaging and commercial aspects such as price and availability. The main parameter left for optimization is thus the receiver's sensitivity, which corresponds with a maximized feedback resistor R_f. According to (3), this is achieved with a maximized open-loop voltage gain A. Equivalently, the maximal bandwidth for a given transimpedance gain is also achieved with a maximized voltage gain. A must thus always be maximized for an optimal receiver.

A. Maximal Voltage Gain in a Transimpedance Amplifier for Telecommunications

Fig. 2(a) is a simple single-stage voltage amplifier. If the loading by the input capacitance C_{next} of the succeeding stage (M_2) is negligible, its gain-bandwidth product is approximately given by

$$GBW_{1s} \approx \frac{g_{m1}}{C_{D1} + C_{next}} \approx \frac{g_{m1}}{C_{D1}}. \quad (4)$$

This is mainly limited by the drain capacitance of M_1 (C_{D1}). For a given transistor length, a factor α can be defined as [2]

$$C_D = \alpha \cdot C_{GS}. \quad (5)$$

This factor is close to unity, although it depends on the technology and the drain bulk voltage (Table I). With (5), (4) can be rewritten as

$$GBW_{1s} = A_{1s} \cdot BW_{1s} \approx \frac{g_{m1}}{\alpha \cdot C_{GS}} = \frac{\omega_T}{\alpha}. \quad (6)$$

A transimpedance amplifier can be compared with a voltage amplifier in unity feedback configuration. The bandwidth of the voltage amplifier determines the second pole in the transimpedance structure. To guarantee stability, this pole has to be a factor X_A higher than receiver's bandwidth, so

$$GBW_{1s} = X_A \cdot BW_{Transamp} \quad (7)$$

with X_A at least two to three depending on the required phase margin [3]. As the transmission speed is determined in telecommunications applications, the maximal achievable gain for a single-stage voltage amplifier used in a transimpedance configuration is derived as

$$A_{1s} = \frac{\omega_T}{\alpha \cdot BW_{1s}} = \frac{\omega_T}{\alpha \cdot X_A \cdot BW_{Transamp}}. \quad (8)$$

Depending on the transmission speed compared with the technology, a multiple-stages approach may display better results [4]. Fig. 2(b) is a simple voltage amplifier with three identical stages. Each stage is loaded by an identical one. The gain bandwidth of an individual stage is given by

$$GBW_{3s,i} = \frac{g_m}{\alpha \cdot C_{GS,i} + C_{GS,i+1}} = \frac{\omega_T}{(1 + \alpha)}. \quad (9)$$

The complete amplifier features a multiple-poles rolloff. To obtain the same phase margin as with a single-stage amplifier, the bandwidth of each individual amplifier stage has to be at

$$BW_{3s,i} = X_3 \cdot X_A \cdot BW_{Transamp} \quad (10)$$

with X_3 approximately three for a three-stage amplifier. By combining (9) and (10), the maximum achievable voltage gain of the three-stage amplifier is given by

$$A_{3s} = A_{3s,i}^3 = \left(\frac{\omega_T}{(1 + \alpha) \cdot X_3 \cdot X_A \cdot BW_{Transamp}}\right)^3. \quad (11)$$

The choice between a single and a multiple-stage approach thus mainly depends on the ratio between the technology's f_t and the transmission speed.

B. The CMOS Feedback Resistor

To guarantee the compatibility with any standard digital CMOS process, the feedback resistor can be replaced by an MOS transistor in its linear region. This offers the supplemental advantage that, if necessary, the resistance value can

$$Z_{cl} \approx \frac{R_f}{1 + s \cdot \left(\frac{C_{in\,T} \cdot R_f}{A} + \frac{C_{out\,T} \cdot R_{out\,A}}{A}\right) + s^2 \cdot \frac{C_{in\,T} \cdot R_f \cdot C_{out\,T} \cdot R_{out\,A}}{A}}. \quad (1)$$
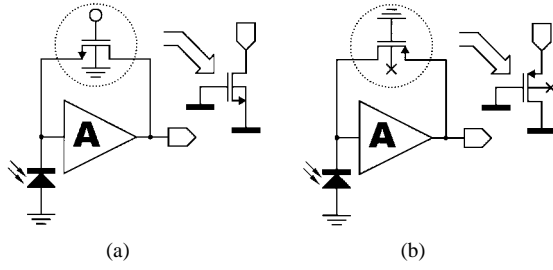
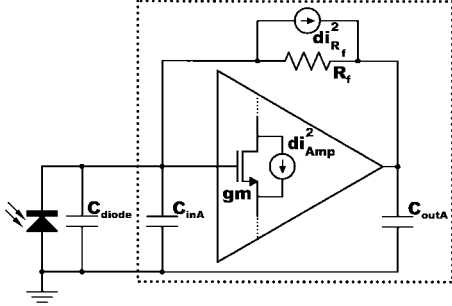Fig. 3. Comparison between (a) an NMOS and (b) a PMOS feedback resistor.

Fig. 4. Main noise contributions of a transimpedance amplifier.

be adjusted simply by changing its gate bias voltage. When the photodiode is connected between input and ground, an NMOS is best avoided [Fig. 3(a)]. As its source is at a virtual ground, a large input current results in a large V_{ds} while V_{gs} is almost constant. The NMOS resistance thus increases with the input current, which results in a reduced dynamic range. The NMOS may even go into saturation for large input currents. For a PMOS resistor, any change in V_{ds} is reflected in an equal change in V_{gs} [Fig. 3(b)]. Due to the virtual ground at the input of the amplifier, the PMOS feedback resistance is actually a parallel circuit of g_m and g_{ds}, so that

$$R_{f\_\mathrm{PMOS}} = \frac{1}{g_{\mathrm{ds},\,\mathrm{PMOS}} + g_{m,\,\mathrm{PMOS}}}. \tag{12}$$

When used in an N-well process, the biasing of the well determines the relative importance of g_m. If it is connected to the power supply, the transistor's V_t is enlarged and V_{dssat} is equally reduced. The transistor is less in its linear region, and g_m becomes relatively more important compared with g_{ds}. As g_m increases with the current, R_{f_PMOS} reduces and dynamic compression is achieved [5]. With the N-well connected to the source, this effect is much less pronounced, and the feedback resistance is practically constant for the input current range of interest. The major disadvantage of this approach is the loading of the transimpedance amplifier's output node with the well capacitance. Furthermore, the signal on the output is capacitively coupled to the bulk via the N-well-to-bulk junction so that noise could be injected into the substrate.

C. Integrated Input-Referred Noise with Limited Feedback Resistor

The noise performance of a transimpedance amplifier is analyzed through the basic circuit of Fig. 4. The resistor's

noise is modeled by its current noise source di^2_{Rf}. The amplifier's noise is concentrated in a single current noise source di^2_{Amp} of an equivalent MOS transistor. In a good design, this is mainly determined by the input transistor. The equivalent input-referred current noise power spectral density is given by

$$\overline{di^2_{\mathrm{eq,\,in}}}(\omega) = \frac{8}{3} \frac{kT}{gm \cdot R_f^2} \cdot |1 + s \cdot R_f \cdot C_{\mathrm{in}\,T}|^2 + 4\frac{kT}{R_f}. \tag{13}$$

The transistor's $1/f$ noise is not considered, as it is only important at frequencies below our interest. For $g_m R_f > 1$, which corresponds with a sufficiently large feedback resistor, (13) is reduced to

$$\overline{di^2_{\mathrm{eq,\,in}}}(\omega) \approx \frac{8}{3} \frac{kT \cdot \omega^2 \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}})^2}{g_m} + 4\frac{kT}{R_f} \tag{14}$$

with C_{gs} being the main contributor to the amplifier's input capacitance. With

$$C_{\mathrm{gs}} \approx \frac{2}{3} \cdot C_{\mathrm{ox}} \cdot W \cdot L$$

and

$$g_m \approx \mu \cdot C_{\mathrm{ox}} \cdot \frac{W}{L} (V_{\mathrm{gs}} - V_t) \tag{15}$$

it can be further simplified to

$$\overline{di^2_{\mathrm{eq,\,in}}}(\omega) \approx \frac{16}{9} \frac{kT \cdot \omega^2 \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}})^2 \cdot L^2}{\mu \cdot C_{\mathrm{gs}} \cdot (V_{\mathrm{gs}} - V_t)} + 4\frac{kT}{R_f}. \tag{16}$$

At low frequencies, the resistor's noise is dominant, while at higher frequencies, the amplifier's noise becomes the largest. It is commonly believed that the best noise performance is always achieved for an amplifier's input capacitance equal to the photodiode's capacitance, or $C_{\mathrm{diode}} = C_{\mathrm{gs}}$ [6]. This conclusion is nevertheless based on the assumption that R_f is independent of C_{gs}, which cannot be guaranteed in high-speed designs. When the required bandwidth is large compared to the technology's capabilities, the achievable feedback resistor is limited (3).

The total integrated input-referred current noise power for a transimpedance amplifier is calculated by integrating (16), taking (3) into account, up to the noise bandwidth, which is assumed to be a factor F_{NB} higher than the receiver's bandwidth. The integrated input-referred current noise power is then given by

$$\begin{aligned}
\overline{i^2_{\mathrm{eq,\,in}}} &\approx \int_{\omega=0}^{\omega=F_{\mathrm{NB}} \cdot BW_{\mathrm{Transamp}}} \frac{16}{9} \\
&\quad \cdot \frac{kT \cdot \omega^2 \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}})^2 \cdot L^2}{\mu \cdot C_{\mathrm{gs}} \cdot (V_{\mathrm{gs}} - V_t)} \\
&\quad + 4\frac{kT \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}}) \cdot BW_{\mathrm{Transamp}}}{A} \\
&= \frac{16}{27} \frac{kT \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}})^2 \cdot L^2}{\mu \cdot C_{\mathrm{gs}} \cdot (V_{\mathrm{gs}} - V_t)} \cdot F_{\mathrm{NB}}^3 BW_{\mathrm{Transamp}}^3 \\
&\quad + 4\frac{kT \cdot (C_{\mathrm{gs}} + C_{\mathrm{diode}})}{A} \cdot F_{\mathrm{NB}} BW_{\mathrm{Transamp}}^2. \tag{17}
\end{aligned}$$

Although the first term contains the receiver's bandwidth to the third power, the second term may not be negligible when

A is small due to the bandwidth requirements. This means that the feedback resistor's noise, which causes the second term, cannot be neglected. To determine the optimal C_{gs} for this case, a factor X_N is defined as

$$X_N = \frac{C_{gs}}{C_{diode}}. \tag{18}$$

This factor is introduced in (17). Its optimal value, which corresponds with the minimal noise, is obtained by differentiating that equation to X_N and solving the result to zero. It is given by

$$X_{N,\,opt} = \frac{1}{\sqrt{1 + \frac{27}{4} \frac{\mu \cdot (V_{gs} - V_t)}{A \cdot L^2 \cdot F_{NB}^2 BW_{Transamp}}}}. \tag{19}$$

The optimal C_{gs} is thus smaller than C_{diode}. The equality is a limit situation that occurs when the second term in the denominator is negligible. For a certain amplifier's bandwidth, the optimal C_{gs} approaches C_{diode} for increasing A and F_{NB}. This is because a high voltage gain allows a large feedback resistor R_f whose noise contribution is inversely proportional to its value. A large F_{NB} corresponds with a noise integration up to high frequencies where the amplifier's noise contribution is dominant. This factor is confined by the voltage amplifier's bandwidth. In a single-stage amplifier, its maximal value is given by

$$F_{NB1,\,max} = \frac{\pi}{2} \cdot X_A. \tag{20}$$

In practical situations, it will, however, be smaller, as the second stage will limit the noise bandwidth. In transimpedance amplifiers based on a single stage's achieving the maximal gain derived in Section II-A, the optimal ratio of C_{gs} to C_{diode} is given by

$$X_{N,\,opt} = \frac{1}{\sqrt{1 + \frac{27}{4} \frac{\mu \cdot X_C \cdot X_A \cdot (V_{gs} - V_t)}{L^2 \cdot F_{NB}^2 \cdot \omega_T}}}. \tag{21}$$

It is plotted in Fig. 5 for typical values of a 0.7-μm technology. Small variations from the optimal value will not affect the noise too much. The knowledge that C_{gs} is smaller than C_{diode} for optimal noise performances is interesting in high-speed designs, as it allows one to reduce the speed-limiting input capacitance without fearing noise degradation.

III. THE 1-Gb/s TRANSIMPEDANCE AMPLIFIER

The 1-Gb/s transimpedance amplifier is presented in Fig. 6. It is based on a g_m/g_m voltage amplifier featuring a high speed combined with an accurate gain. In the 0.7-μm CMOS technology, the maximal voltage gain for a 500-MHz closed-loop bandwidth, required for a 1-Gb/s nonreturn-to-zero-coded data rate, is achieved with a single stage. The amplifier's second pole is placed at approximately 1.5 GHz. An optimized voltage gain larger than two is achieved, which corresponds to a gain-bandwidth product of over 3 GHz.

The receiver is designed for a total photodiode capacitance of 800 fF at its input. This includes both the diode and the
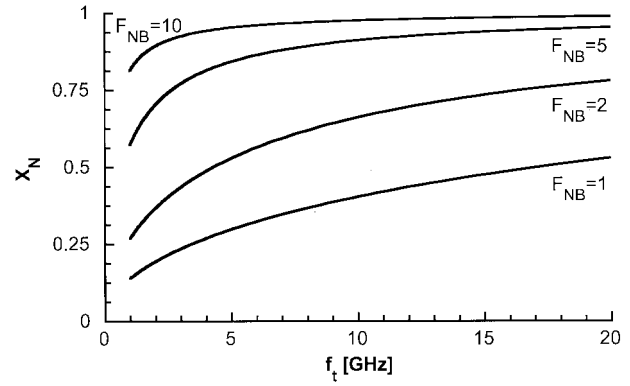

Fig. 5. Optimal C_{gs}/C_{diode} for various F and f_t 0.7-μm CMOS, $\alpha = 1$, $X_A = 2.5$, $V_{gs} - V_t = 200$ mV.
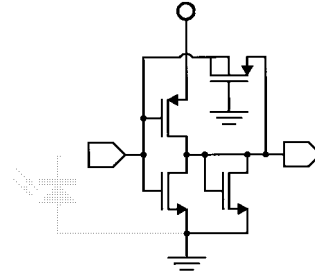

Fig. 6. A 1-Gb/s transimpedance preamplifier.

bondpad capacitance. It is sufficient for the use of an external commercial diode. The transimpedance amplifier is loaded by a postamplifier integrated on the same chip and described in Section IV. The careful design and layout of this stage limits its capacitive loading to 80 fF. According to (3), a 1-kΩ feedback resistor can be implemented. It is realized as a PMOS transistor. Its well is connected to the drain. This is permitted, as the signal on the output node is sufficiently small due to the small input current. The well capacitance is now added to the input node, which already includes the large photodiode's capacitance. This results in only a small bandwidth degradation. Furthermore, as the input's node is a virtual ground, no noise is injected into the substrate. The amplifier consumes about 5 mA from the 5-V power supply.

IV. THE POSTAMPLIFIER

To obtain a completely integrable optical receiver, the preamplifier's output signal is further amplified to a rail-to-rail voltage. A postamplifier, based on a string of modified inverters biased at their threshold voltage, is used for this. The first inverters have a small input signal and act as linear amplifiers. At the end of the chain, clipping occurs at the ground and power-supply voltage. The advantage of this approach is that the exact serial number of the inverter where the clipping begins in the chain is irrelevant. A larger input signal will simply result in a shift forward of the first clipping. This results in a large dynamic range without automatic gain control. The major challenge for the practical realization of the chain is the correct biasing of the inverters. It is done with an
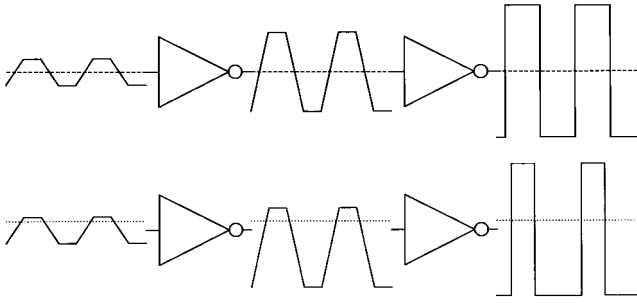
Fig. 7. Signal degradation due to the nonoptimal biasing of the inverter chain.
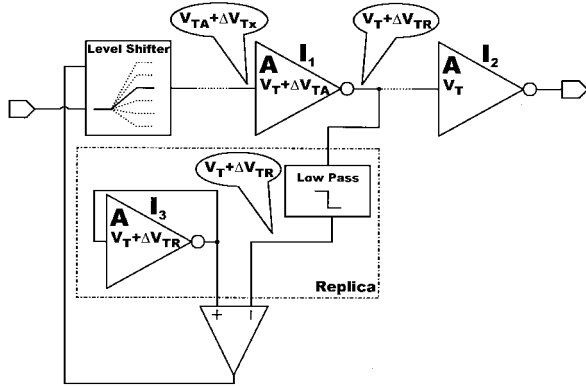

Fig. 8. Replica biasing with mismatch compensation principle.

offset-tolerant replica biasing circuit with accurate threshold control.

A. Offset-Tolerant Replica Biasing with Accurate Threshold Control

In all replica biasing schemes, there is inevitably some offset between the desired bias voltage and that actually obtained through the replica. This is due to mismatches between the actual circuit and its replica. For the presented inverter chain, it results in a nonoptimal biasing of the first inverter and leads to a degeneration of the duty cycle of the signal, which is inversely proportional to the signal's amplitude (Fig. 7). By adding a supplemental gain stage in the replica loop before the biased inverter, the effect of mismatch is reduced as the signal swing is enlarged. This is the principle of the offset-tolerant replica biasing circuit presented in Fig. 8. In this scheme, the biasing of inverter I2 is forced to the threshold voltage of its replica (I3). The extra foregoing gain A is provided by inverter I1. As it is included in the replica feedback loop, it is biased accurately, as will be demonstrated.

The replica feedback loop consists of a level shifter and an inverter (I1) in the signal path and a low-pass filter, a replica (I3) of inverter I2 and a comparator alongside. The dc bias voltage at the input of the first out-of-the-loop inverter (I2) is compared with the replica's threshold and forced to this voltage by adjusting the level shifter. Due to various effects as process or temperature varies, there is an offset $\Delta V_{\rm TR}$ between the threshold voltages of inverter I2 and its replica I3. I2 is thus not perfectly biased. However, as the signal has
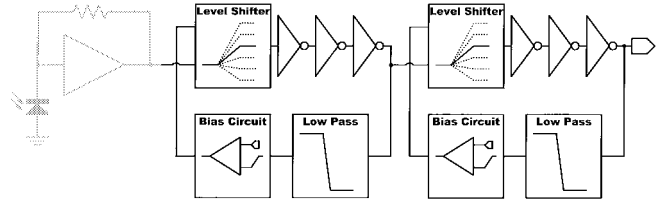
been boosted by I1, its alteration by I2 is limited. The small signal is now present at the input of I1, and consequently this must be biased very accurately. If I1 has a threshold voltage $V_{\rm TA} = V_T + \Delta V_{\rm TA}$, its input biasing is forced to $V_{\rm TA} + \Delta V_{\rm Tx}$ by the feedback loop. The standard deviation on this biasing error is given by

$$\sigma^2(\Delta V_{\rm Tx}) \approx \frac{\sigma^2(\Delta V_{\rm TR}) + \sigma^2(\Delta V_{\rm TA})}{A_I^2} \qquad (22)$$

with A_I the gain of I_1. It can be reduced by enlarging A_I. Eventually, several inverters may be cascaded in the loop to achieve this. The absolute offset limitation is shifted to the first out-of-the-loop inverter, where its effect is minimal, as the signal is relatively large there.

As part of the signal path is included in the feedback loop, any dc in the data signal will be suppressed. The minimal tolerated input frequency is thus restrained. If necessary, however, the data can be scrambled to raise its minimal frequency component. A major challenge to realize the offset-tolerant biasing lies in the stability of the feedback loop with its large loop gain. Hereto, a low-frequency pole is introduced outside the signal path. This is not boundless, especially in an integrated environment with no large capacitors.

B. Realization of the Postamplifier

The presented optical receiver comprises a double replica biased inverter string (Fig. 9). Both feedback loops consist of five inverting stages: three modified inverters, the comparator, and the level shifter, which also performs an extra inversion. The multiple-inverter approach is necessary as the gain of each stage is limited due to the high bandwidth. The bandwidth of the inverters in the signal-path portion of the replica loops must be sufficient to avoid dc shifts due to frequency components larger than their -3-dB frequency. The bias circuit would indeed compensate this, resulting in a degraded biasing. As multiple inverters are cascaded in each loop, their bandwidths must be sufficiently larger than the signal's bandwidth. They are designed with a 1.5-GHz bandwidth. Standard inverters do not achieve such a high small-signal bandwidth due to their large gain. By limiting it, the bandwidth is boosted. The modified high-speed inverter is presented in Fig. 10(a). An NMOS diode-coupled transistor (M_3) limits the gain. It is preferred over a PMOS, as it is smaller for a given g_m. The diode is connected between the power supply and the output node. The current it consumes is drained through an NMOS transistor (M_1), which grows less than if the PMOS transistor (M_2) had to drain the extra current. Furthermore, the bulk effect due to the nonzero $V_{\rm BS}$ of the diode (M_3)
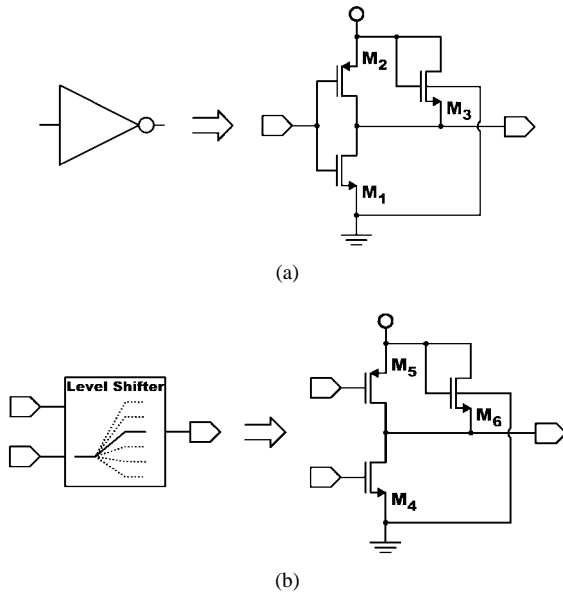

Fig. 9. Block scheme of the postamplifier.

Fig. 10. (a) High-speed inverter and (b) high-speed level shifter.
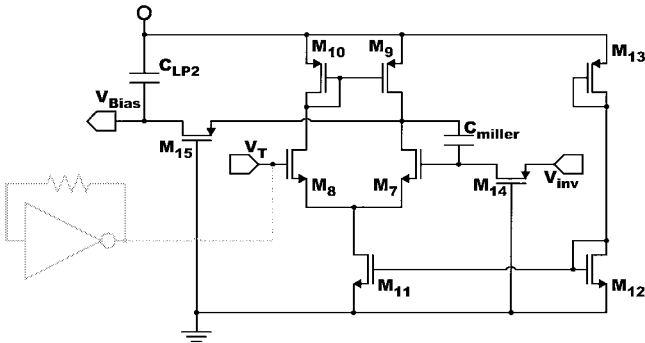

Fig. 11. OTA comparator with low-pass filter.

enhances its g_m, which reduces its required size even more. These effects result in a minimal increased capacitive loading of the basic inverter and thus in a higher speed than with another configuration. As both level shifters are in the signal path too, their bandwidth must be comparable to that of the inverters. They are based on the same topology [Fig. 10(a)]. The signal to the shifter is applied to the input NMOS (M_4), while the PMOS (M_5) controls the shifting. Notice that the shifter serves both as a level shifter and as an inverting small-signal amplifier, although with limited gain.

The low-pass filter and the comparator complete the replica feedback loop (Fig. 11). The filter measures the dc voltage at the input of the first out-of-the-loop inverter. This is compared to the replica's threshold by the comparator and adjusted through the loop. As the combined gain of the cascaded high-speed inverters in the signal-path portion of the loop is high at the receiver's bandwidth, the filter's corner frequency has to be sufficiently low to ensure stability. It also determines the minimal input signal frequency that can be amplified by the receiver. Unfortunately, lowering the corner frequency also augments the settling time. If necessary, this can be shortened by a dc-level measurement technique based on peak detection [7].
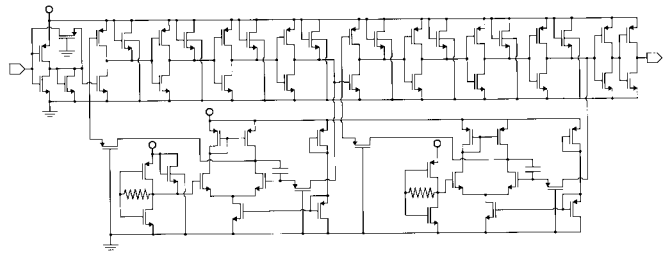

Fig. 12. Circuit diagram of the complete receiver.

The low-pass filter is basically an RC filter. The 280-kΩ resistor is replaced by a PMOS transistor in its linear region. To obtain a very low pole, the 10-pF capacitor C_{miller} is boosted by placing it in a Miller configuration, with the comparator as gain element. This results in a corner frequency of 500 Hz. The comparator is based on a simple operational transconductance amplifier (OTA) structure with a dc gain of 120 and a bandwidth of 45 kHz. Its input transistors are sized to avoid a systematical offset. It consumes 155 μA from the single 5-V power supply. The output voltage of the OTA biases the level shifter through a second low-pass filter that compensates the zero introduced by the Miller capacitance. This second filter consists of a 220-kΩ PMOS resistor (M_{15}) and a 5-pF capacitor. Note that this is a capacitor to the power supply to keep the V_{gs} of the level shifter's bias-input PMOS transistor constant.

V. REALIZATION OF THE COMPLETE 1-Gb/s RECEIVER

The circuit schematic of the complete 1-Gb/s receiver is presented in Fig. 12. It has been realized in a standard 0.7-μm CMOS technology. All circuit elements, including decoupling capacitors and resistors, are integrated on the die. Consequently, except from a photodiode, no external components are required to complete the optical receiver. A digital buffer string is implemented subsequent to the receiver. It buffers the output signal to ease the measurements. The first inverter in that string is minimal and driven by the receiver with a full rail-to-rail swing. The subsequent inverters are scaled up to enlarge the current driving capabilities to drive the 50-Ω measurement instruments. Fig. 13 is a microphotograph of the receiver. Several bondpads were introduced on the layout to monitor the dc voltages of both postamplifiers. These bondpads are only meant for measurement purposes and can be omitted in the definitive receiver.

VI. MEASUREMENTS ON THE 1-Gb/s RECEIVER

The receiver is mounted on a ceramic substrate for the measurements. This provides separate, decoupled power supplies for the analog and the digital part. No supplemental external biasing voltages or currents nor any supplementary external decoupling of the biasing points are applied. Actually, the extra bondpads provided for dc measurements are left unconnected on the die during the dynamic measurements.

The optical receiver is characterized electrically by replacing the photodiode, which can be modeled as a high-ohmic current source, by its Thevenin equivalent. A large series
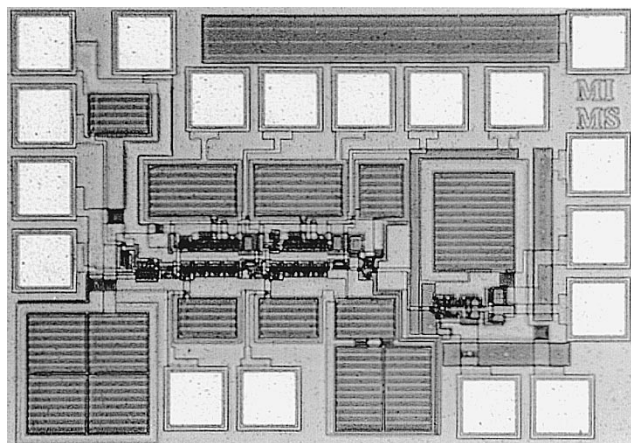
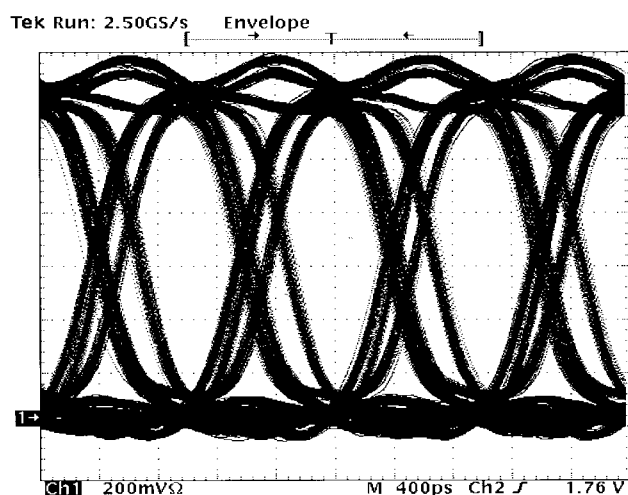Fig. 13. Microphotograph of the 0.7-μm, 1-Gb/s optical receiver.

Fig. 14. Measured eye diagram of the optical receiver at 1 Gb/s.

resistor is inserted between the 50-Ω signal source's output and the receiver's input. The photodiode's capacitance is modeled by a 500-fF capacitor. It adds up to the receiver's input bondpad capacitance to a total of 800 fF. The transimpedance amplifier consumes approximately 5 mA from a single 5-V power supply. It achieves a 1-kΩ transimpedance gain. The corresponding input-referred current noise spectral density is smaller than 7 pA/$\sqrt{\text{Hz}}$ from 1 to 500 MHz. The complete optical receiver, including transimpedance amplifier and postamplifiers with their biasing circuits and replicas, consumes approximately 20 mA from the single 5-V power supply. The output of the circuit is coupled directly to the 50-Ω input of a digital oscilloscope. Although the internal data signal reaches full digital levels, the output buffer was not designed to drive 50 Ω up to 5 V. The measured output signal is therefore scaled down to approximately 1 V. Fig. 14 shows a measured eye diagram at 1-Gb/s throughput. A sensitivity of better than 10 μA has been measured. When powered at

a 3.3-V supply, the circuit consumes 8 mA and features a maximal speed of 600 Mb/s.

VII. CONCLUSION

High-speed integrated optical communication systems tend to gain in importance. This paper has presented such a receiver in CMOS. Various design consideration of a transimpedance amplifier have been discussed. A biased inverter string with an offset-tolerant replica biasing circuit was proposed to perform the postamplification up to a full rail-to-rail voltage. The circuits were used to realize a 1-Gb/s optical receiver in a standard 0.7-μm CMOS. The circuit features a 1-kΩ transimpedance gain for an 800-fF photodiode in the first stage and a full rail-to-rail output voltage. A sensitivity of better than 10 μA was achieved. The circuit demonstrates the importance of CMOS in future communication links. Full integration, high gain, high sensitivity, and a speed in the gigabit area are compatible with CMOS technologies.

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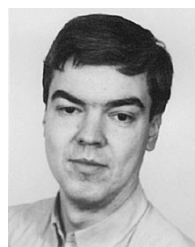
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Michel S. J. Steyaert (S'85–A'89–SM'92), for a photograph and biography, see this issue, p. 911.