CONTROL AND SIGNAL PROCESSING FOR LITHOGRAPHY

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Contents

Summary

This thesis investigates the application of advanced control and signal processing methods to improve lithography performances.

Warped wafers affect the various baking processes in lithography. Further, warpage can result in substantial spatial variation in critical dimension (CD). A real-time temperature control method was proposed for post-exposure bake of resist. It was demonstrated experimentally that real-time control of bake plate temperature to give nonuniform temperature distribution across warped wafer can reduce within-wafer and wafer-to-wafer CD variation.

Resist thickness is nonuniform after spin coating (Decre and Vromans, 2000). Nonuniform CD is expected due to the standing wave effects. A real time control method was presented to improve thickness and CD uniformity. Resist thickness was monitored with a spectrometer during post-apply bake, and controlled by manipulating the heating power of bake plate in real-time. Experimental results showed that the thickness nonuniformity was reduced to less than 1nm and CD deviation was reduced to about 2nm.

To improve repeatability for the wafer thermal processing, a multizone feed-forward controller was proposed. The objective is to reject the disturbance caused by placement of a cold wafer on the bake plate. The optimal feed-forward control signals can be obtained by solving a linear programming problem. Experimental results showed that the disturbance would be reduced to less than 0.1°C.

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivations

1.1.1 Critical Dimension Control in Lithography

Semiconductor manufacturing has greatly affected the world due to the wide application of semiconductor devices. The industry development can basically be symbolized by the so called integrated circuit (IC) scaling. The number of transistors on a single IC doubles every two years according to Moore's law (Hamilton, 2003). Critical dimension (CD) of patterns is currently below 100nm. A more stringent demand on the CD variation is imposed. By the year 2010, a CD control requirement of 4.7nm is expected for 45nm technology node (*International Technology Roadmap for Semiconductors, SIA*, 2005). The industry has moved through several lithography generations to achieve smaller feature sizes. However, technology

transition is expensive and time consuming. To reduce cost, a better way is to extend the life cycle of current lithography generation. The challenge is to maintain CD variations within the desired specifications while pushing feature size to its absolute minimum achievable value. One solution is the introduction of advanced equipment and process control (Moynes, 2006; Miyagi *et al.*, 2006). This thesis will investigate the application of advanced control and signal processing to meet some stringent requirements for CD control in lithography.

CD control is required for obtaining adequate transistor, interconnect and consequently overall circuit performance (Edgar *et al.*, 2000). As shown in Figure 1.1, a typical lithography includes resist coating, post-apply bake (or softbake), exposure, post-exposure bake (PEB), development, and an optional post development bake. The sensitivity of the process to small variations in photoresist coating, exposure dose and the bake plate temperature can result in the final CD going out of specifications.

Identification of the main sources of CD variations will help define the path to improving CD control (Postnikov *et al.*, 2003). The CD is significantly impacted by several variables (Kim *et al.*, 2004). Exposure was regarded as an important source for CD variation (Postnikov *et al.*, 2003), and the errors may originate from exposure dose (Asano *et al.*, 2002; Kotera *et al.*, 2005), grid size (Lee *et al.*, 2004*a*), and illumination conditions (Ha *et al.*, 2003). Anther major source of CD variation is the thermal processing in lithography, such as PEB (Li, 2001; Cain *et al.*, 2005), and post-apply bake (Raptis, 2001). Each of the bake steps serves different roles in transferring the desired patterns into the substrate (Suzuki and Smith, 2007). The

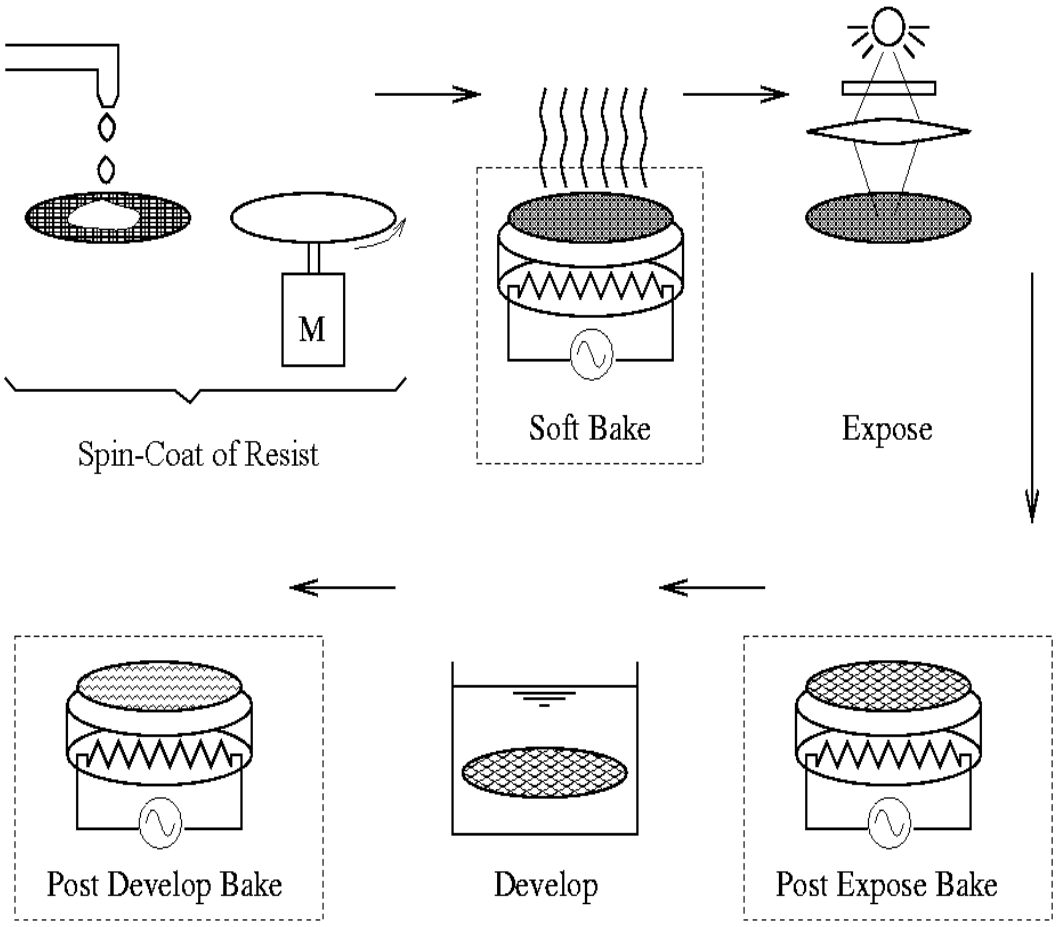


Fig. 1.1. Steps of Lithography.

principal objective of this thesis is to improve CD uniformity by applying real-time control approaches in the various thermal processes.

1.1.2 Post-Exposure Bake and Warpage Effects

Optical lithography has been the mainstream technology for volume manufacturing since the earliest days of the microelectronics industry. In optical lithography techniques such as chemical amplification are necessary in order to make photoresists sensitive enough to achieve wafer throughput goals for manufacturing. In most chemically amplified resists (CARs), the chemical amplification process is

driven by the PEB step. Therefore, CD is highly sensitive to PEB temperature. For commercially available CARs, a representative PEB latitude for CD variation is about 5∼20 nm/°C (Seegar, 1997). Temperature sensitivity of 193nm CARs photoresist is in the order of 7∼10nm/°C (Friedberg *et al.*, 2004). Nordquist *et al.* (2000) and Berger *et al.* (2004*a*) reported a representative sensitivity of 8 nm/°C for commercially available deep ultraviolet (DUV) resists.

Due to the high sensitivity of CD to PEB temperature, CD can be controlled by manipulating the PEB process. Achieving CD uniformity is one of the major concerns. Zhang *et al.* (2004) successfully compensated systematic CD variation across wafers by adjusting the PEB baking profiles on different parts of wafers through a multizone bake plate. Lee *et al.* (2004*b*) reduced CD variation from 4.8nm 3σ to 3.9nm 3σ using a 25-zone bake plate. A similar study (Berger *et al.*, 2004*a*) reduced the CD variation from 8.9nm to 6.7nm. These methods are usually implemented through a run-to-run mode and have proved to be effective in eliminating systematic errors. In run-to-run control method, the information from previous wafer or patch is used for control of the current wafer or batch. In the presence of random variation, however, the run-to-run methods become less effective (Xu *et al.*, 2002).

Warpage is one challenge for PEB processing of wafers (Bhattacharya *et al.*, 2000; Banerji *et al.*, 2005). One factor that contributed to warpage was stress (Fukui *et al.*, 1997). El-Awady (2000) studied the influences of warpage on baking temperature, and gave quantitative results as 1°C change for a warpage level of 50 μm

through simulation studies. Such variation will cause substantial CD nonuniformity.

Since warpage is usually different wafer-to-wafer, measurement of warpage is essential for CD nonuniformity compensation. The warpage can be measured by various methods (Yang *et al.*, 2006). The shadow and projection Moire techniques are widely used warpage measurement methods (Ding *et al.*, 2002; Powell and Ume, 2007). Warpage can also be measured through capacitive probes (Fauque, 2001) and through the pneumatic-electromechanical effects (Fauque and Linder, 1998). All these methods have the advantage that they can give the precise profile of the warped wafer. However, one disadvantage is that they are off-line and need extra processing time to obtain the warpage information. Further, the delay between the exposure and the PEB steps needs to be reduced due to post-exposure delay effect of chemically amplified resists (Lee *et al.*, 2001). This would eliminate any time consuming measurement between these two steps.

One objective of this thesis is to adopt an in-situ warpage detection method for proper PEB processing of warped wafers to obtain CD uniformity.

1.1.3 Post-Apply Bake Effects and Resist Thickness Control

Besides PEB, post-apply bake is another important baking process. During post-apply bake, residual solvent evaporates and leaves empty volume behind, which is relaxed immediately, resulting in film thickness reduction (Tortai, 2004). For

Shipley UV3, a theoretical model of the thickness variation during post-apply bake was developed and matched well with experimental data (Hsu *et al.*, 2001). It was found that the rate of solvent removal was controlled by its diffusion, which was affected by post-apply bake temperature in an Arrhenius mode. Thus the post-apply bake temperature and time will affect the final resist thickness.

Lithography properties vary as a sinusoidal function of resist thickness due to the the standing wave effects, or swing curve effects. The swing curve effects for an alternating phase shift mask were reported by Singh *et al.* (2006). CD swing curves were represented in two dimension to optimize lithography performance (Schiltz and Schiavone, 2000). Thus, optimizing the post-apply bake process is crucial to obtain uniform lithography latitude, such as CD. Lithographic performance were enhanced for two negative chemically amplified resists by adjusting post-apply bake time (Raptis, 2001). Lee *et al.* (2002) demonstrated that an within-wafer thickness nonuniformity of less than 1nm can be obtained by manipulating the processing temperature during post-apply bake for an i-line resist Shipley 3612. One goal of this thesis is to obtain resist thickness and CD uniformity by real-time control of post-apply bake processing.

1.2 Contributions

In this thesis, the application of advanced metrology, control and signal processing algorithms to meet some stringent requirements in lithography is investigated. This thesis will address three areas: 1) CD uniformity improvement by real-time

temperature control for warped wafers during PEB, 2) CD uniformity improvement via real-time resist thickness control in the post-apply bake and 3) optimal feed-forward control for thermal processing of wafers to improve repeatability.

1.2.1 CD Uniformity Improvement by Real-Time Temperature Control

During thermal processing, a wafer at room temperature is dropped onto the bake plate maintained at a set point temperature with a feedback controller. The proximity pins produce an air-gap between the wafer and the bake plate to avoid contamination. For flat wafers, this air-gap equals to the pin length as shown in Figure 1.2(a). For warped wafers, however, the air-gap will be bigger (upward warpage) or smaller (downward warpage) as shown in Figure 1.2(b). Wafer temperature will be different also. The bigger the air-gap, the lower the wafer temperature.

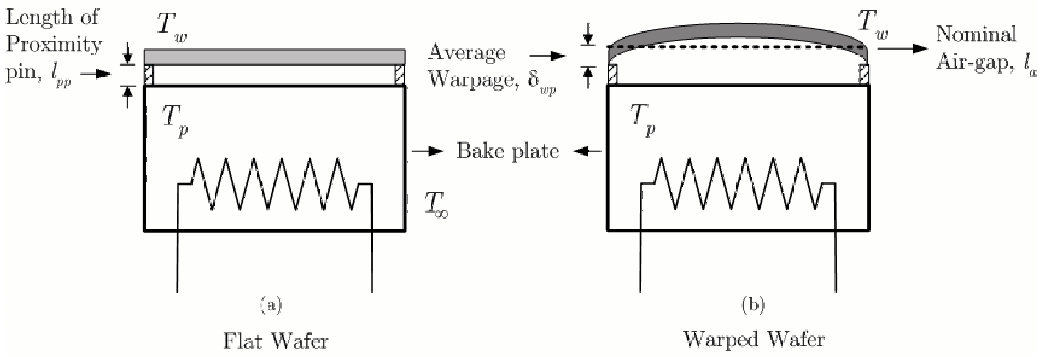


Fig. 1.2. Schematic diagram of the baking process.

A real-time temperature control method will be proposed to improve CD uniformity for warped wafers. It is noted that bake plate temperature will drop to

a maximum value before recovering to the set point. It is also noted that flat wafer and warped wafer give different maximum temperature drop as shown in Figure 1.3, solid line and dashed line respectively. Thus wafer warpage can be detected from the maximum temperature drop. Once the warpage is detected, the bake plate temperature can be adjusted in real-time accordingly to reduce wafer temperature variations, as shown by the dash-dotted line in Figure 1.3. CD variations caused by warpage can be compensated before it is formed in the resist. The wafer-to-wafer CD variation compensation will be demonstrated experimentally.

There are also temperature and CD nonuniformity across the wafer due to the different air-gap at different location. To realize within-wafer CD uniformity, a multizone bake plate is used, with the capability to bake different zones to different temperature independently. When the maximum temperature drops of different bake plate zones are recorded, the warpage can be detected. Bake plate temperature for different zones can be adjusted independently to compensate for the wafer temperature and CD variations. The method will be demonstrated experimentally.

1.2.2 CD Uniformity via Real-Time Resist Thickness Control

Resist thickness is another major source for CD nonuniformity. Photoresist is typically spin coated on the wafer to form a thin film. Resist thickness is nonuniform after spin-coating. Nonuniform CDs are expected and they vary as a swing

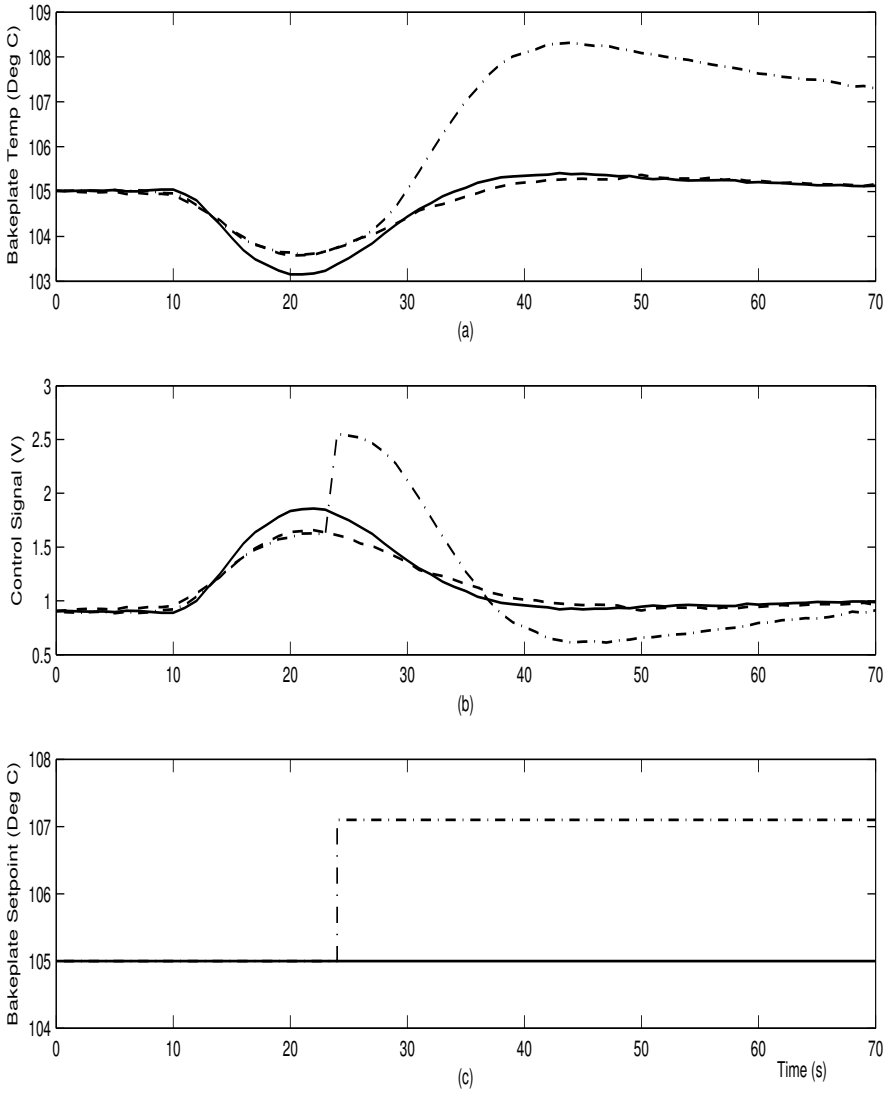


Fig. 1.3. Post-exposure bake temperature and power. Solid line: Flat Wafer; Dashed line: Warped wafer; Dash-dotted line: Warped wafer with setpoint adjustment.

curve function of photoresist thickness due to the standing wave effects. Both wafer-to-wafer and within-wafer variations exist in practice.

In this thesis, a real-time resist thickness control method will be proposed to improve resist thickness and CD uniformity. During post-apply bake, resist thickness reduces gradually due to solvent removal and different temperature gives different thickness reduction. For conventional post-apply bake, the bake plate temperature is maintained at a constant value. The resist thickness nonuniformity remains at the end of the bake. In the method, a spectrometer is used to monitor the resist thickness above the wafer during the post-apply bake. The thickness can be controlled to follow a pre-determined trajectory by adjusting the heating power of the bake plate in real-time. It is to be demonstrated experimentally that both wafer-to-wafer and within-wafer resist thickness nonuniformity of less than 1nm and CD nonuniformity of around 2nm are achieved.

1.2.3 Optimal Feed-Forward Control for Thermal Processing of Wafers

During thermal processing of wafers, it is extremely important to control the temperature within a tight tolerance during the whole bake cycle. When a wafer at ambient temperature is placed onto the hot bake plate, the bake plate endures a sudden drop in temperature due to the heat transferred from the bake plate to the cold wafer. Bake plate controller will adjust the heating power to regulate the

temperature to the setpoint. In automated wafer fab, the next wafer arrives immediately after the baking of the previous wafer. If the processing time is short than the recovery time of the bake plate, the bake plate temperature trajectory will be different from wafer to wafer. Thus it is important to reject the load disturbance effectively to ensure process repeatability.

In this thesis, a multizone optimal feed-forward control strategy is proposed to eliminate disturbance induced by placement of the cold substrate. The disturbance minimization problem is transformed into a linear programming problem with constrains. Thus optimal feed-forward control signals could be obtained by solving the linear programming problem. Using the proposed optimal controller, a disturbance of less than 0.1°C is obtained experimentally.

1.3 Organization

This thesis consists of 5 chapters and is organized as follows. Chapter 2 describes a real-time temperature control method for warped wafers during PEB to improve CD uniformity. The implementation will be discussed in detail for a double-zone bake plate and briefly for a one-zone bake plate. Chapter 3 presents a real-time thickness control method to improve wafer-to-wafer and within-wafer thickness and CD uniformity. An optimal feed-forward control for multizone baking in lithography is proposed and implemented in Chapter 4. Chapter 5 summarizes the research works and gives recommendations for future works.

Chapter 2

CD and Real-Time Temperature Control for Warped Wafers

This Chapter discusses the experimental results on Critical Dimension (CD) control via real-time temperature control for warped wafers. As opposed to run-to-run control where information from the previous wafer or batch is used for control of the current wafer or batch, the approach here is real-time and make use of current information for control of the current wafer CD. In this Chapter it is demonstrated that real-time control of the post-exposure bake temperature to give nonuniform temperature distribution across the warped wafer can reduce CD nonuniformity across the wafer.

2.1 Introduction

The key output in photolithography is the linewidth of the photoresist pattern or CD and the CD is significantly impacted by several variables that must also be monitored to ensure quality (May and Spanos, 2006; Postnikov *et al.*, 2003).

Thermal processing of semiconductor substrate is common and critical in the photolithography sequence. Temperature uniformity control is an important issue with stringent specifications and has a significant impact on the CD (Quirk and Serda, 2001; Narasimhan and Ramanan, 2004; Zhang *et al.*, 2005). The most temperature sensitive step in the photolithography sequence is the post-exposure bake step. As the photolithography industry moves to bigger substrate and smaller CD, the stringent requirements for post-exposure bake processing still persist (Kagerer *et al.*, 2006). For commercially available deep ultraviolet resist, a representative post-exposure bake latitude for CD variation is 8 nm/°C (Nordquist *et al.*, 2000; Berger *et al.*, 2004*a*). A number of recent investigations also showed the importance of proper bake plate operation on CD control (Zhang *et al.*, 2005; Steele *et al.*, 2002; Hisai *et al.*, 2002).

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake plate for a given period of time. The heated bake plate is usually held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake plate near the surface. The wafers are usually placed on proximity pins of the order of 100 μm to create an air-gap to minimize contamination.

When a flat wafer at room temperature was placed on the bake plate, the temperature of the bake plate dropped at first but recovered gradually because of closed-loop control as shown in Figure 2.1 (a). One challenge for thermal processing of wafers in photolithography is the warpage (Bhattacharya *et al.*, 2000). Figure 2.2 (a) shows the bake plate temperature when a wafer warped 140μm center-to-edge was dropped on the bake plate. By comparing Figures 2.1 (a) and 2.2(a), it can be seen that a flat and warped wafer gave rise to different magnitudes of bake plate temperature drops due to different air-gap sizes and hence different thermal resistances between the substrates and bake plate. Figure 2.3 shows a flat and warped wafer on the bake plate. Compared with the flat wafer, because the air-gaps between the warped wafer and bake plate were bigger (smaller), the maximum temperature drops at the bake plate were smaller (bigger). Furthermore, the warped wafer is expected to be heated to a lower (higher) temperature than the flat wafer. Finally, because of nonuniform processing condition, CD across the warped wafer was also not expected to be uniform.

It was demonstrated in Ho *et al.* (2004) and Tay *et al.* (2007*a*) that the air-gap size can be estimated from the maximum bake plate temperature drop through their inverse relationship. It was further demonstrated in Tay *et al.* (2007*a*) that using the heat transfer model of the baking system and the estimated air-gap, the bake plate temperature can be calculated to give uniform temperatures across the warped wafer. In this Chapter the results are extended by demonstrating that real-time control of the post-exposure bake temperature to give nonuniform temperature distribution across the warped wafer can reduce CD nonuniformity.

It was demonstrated that uniform wafer temperature would not assure uniform CD. Instead, nonuniform wafer temperature profile to achieve uniform CD can be derived from the CD and wafer temperature sensitivity. The proposed solution is to adjust the bake plate temperature setpoints on-line and in real-time once warpage is detected to give desired nonuniform wafer temperature profile. Warpage can differ from wafer-to-wafer and hence not expected to be repeatable. If warpage was repeatable then bake plate setpoints could have been fixed. A thermal model is required to relate warpage to the maximum bake plate temperature drops, and to relate the wafer temperature profile and the bake plate temperature profile. The thermal model will be derived in next section.

2.2 Thermal Modeling of the Baking Process

The distributed thermal processing system used in this work consisted of two heating zones, center and edge as shown in Figure 2.3. l_{a1} and l_{a2} represent the average air-gap of the center zone and edge zone respectively. Embedded within each of the heating zones were resistive heating elements and temperature sensors. The zones were separated by a small air-gap of approximately 1 mm for thermal insulation.

Spatial distributions of temperature and other quantities in a silicon wafer are most naturally expressed in a cylindrical coordinate system. It is assumed that the substrate used for baking is a silicon wafer and the bake plate is cylindrical in shape with the same diameter as the wafer. Energy balances on the wafer and

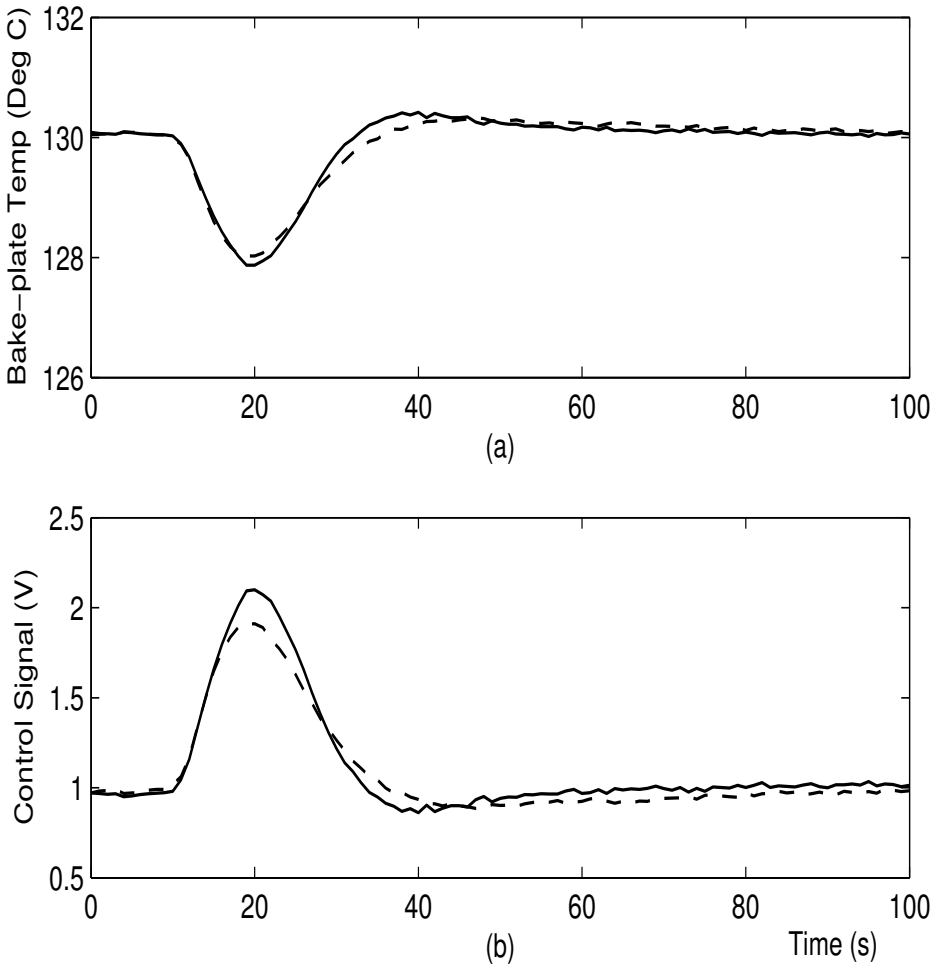


Fig. 2.1. Baking of Flat Wafer 1. Solid-line: center; Dashed-line: edge.

bake plate can be carried out to obtain a two dimensional model as follows.

$$C_{w1}\dot{T}_{w1}(t) = \frac{T_{p1}(t)-T_{w1}(t)}{R_{a1}} + \frac{T_{w2}(t)-T_{w1}(t)}{R_{w12}} - \frac{T_{w1}(t)}{R_{w1}} \quad (2.1)$$

$$C_{w2}\dot{T}_{w2}(t) = \frac{T_{p2}(t)-T_{w2}(t)}{R_{a2}} + \frac{T_{w1}(t)-T_{w2}(t)}{R_{w12}} - \frac{T_{w2}(t)}{R_{w2}} \quad (2.2)$$

$$C_{p1}\dot{T}_{p1}(t) = u_1(t) + \frac{T_{p2}(t)-T_{p1}(t)}{R_{p12}} + \frac{T_{w1}(t)-T_{p1}(t)}{R_{a1}} - \frac{T_{p1}(t)}{R_{p1}} \quad (2.3)$$

$$C_{p2}\dot{T}_{p2}(t) = u_2(t) + \frac{T_{p1}(t)-T_{p2}(t)}{R_{p12}} + \frac{T_{w2}(t)-T_{p2}(t)}{R_{a2}} - \frac{T_{p2}(t)}{R_{p2}} \quad (2.4)$$

where subscripts p, w, a, 1 and 2 denote bake plate, wafer, air-gap, center zone and edge zone respectively. Temperature above ambient, thermal capacitance and

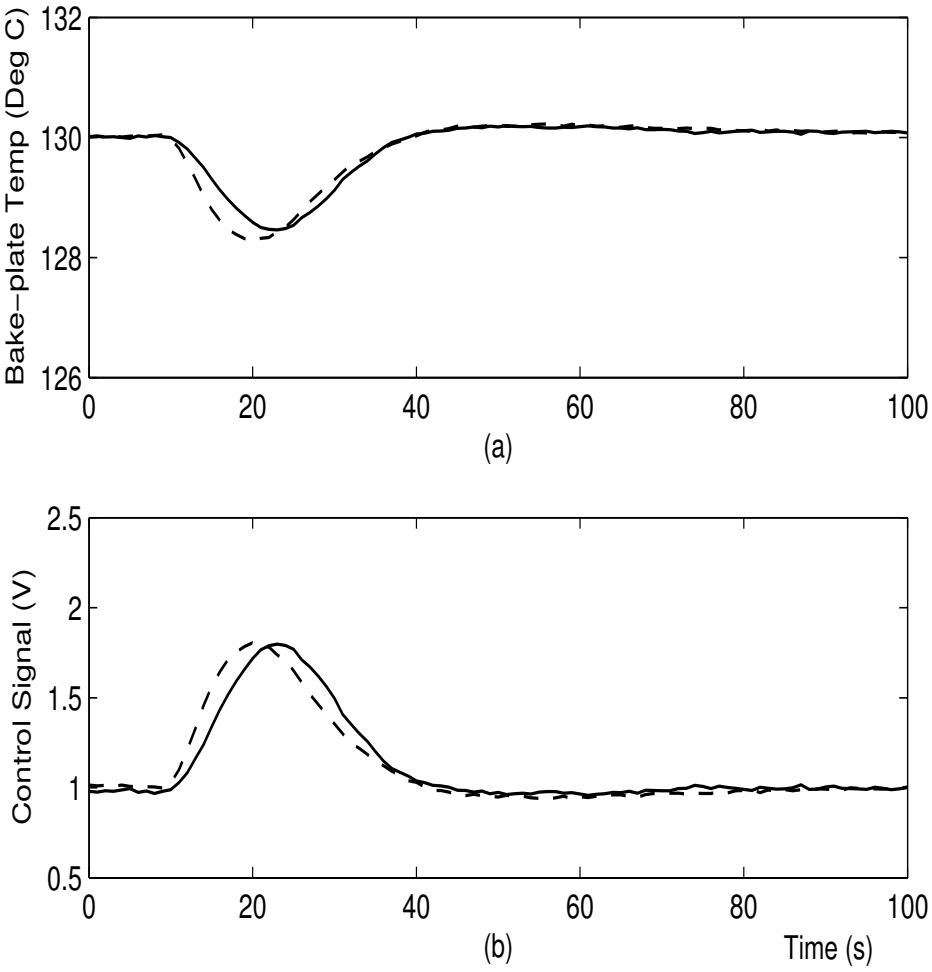


Fig. 2.2. Baking of Warped Wafer 4. Solid-line: center; Dashed-line: edge.

resistance are given by T, C and R respectively. Thermophysical properties of silicon and air can be obtained from handbooks (Raznjevic, 1976) as tabulated in Table 2.1 and standard heat transfer experiments (Ho *et al.*, 2004; Tay *et al.*, 2007*a*) can be conducted to determine most of the thermal capacitance and resistance values in Table 2.2.

Table 2.1. Thermophysical Properties

	Property	Value
Wafer (silicon)	Density, ρ_w	2330 kg/m^3
	Specific heat capacity, c_w	850 J/kgK
	Diameter, d	100 mm
	Thickness, t_w	500 μm
Bake plate	center zone radius, r_1	30 mm
	edge zone radius, r_2	50 mm
Air	Thermal conductivity, k_a	0.03 W/mK
	Convective heat transfer coefficient, h	8 W/m^{2}K

Table 2.2. Thermal Capacitances and Resistances

Thermal Capacitance & Resistance	Value	
R_{p1}	22.2 K/W	experimental
R_{p2}	6.3 K/W	experimental
R_{p12}	16.08 K/W	experimental
R_{w1}	44.21 K/W	$\frac{1}{h\pi r_1^2}$
R_{w2}	24.11 K/W	$\frac{1}{h\pi\left(r_2^2-r_1^2+dt_w\right)}$
R_{w12}	9.52 K/W	experimental
R_{a1}	changes with warpage	$\frac{l_{a1}}{k_a\pi r_1^2}$
R_{a2}	changes with warpage	$\frac{l_{a2}}{k_a\pi\left(r_2^2-r_1^2\right)}$
C_{p1}	101.2 J/K	experimental
C_{p2}	165.8 J/K	experimental
C_{w1}	2.8 J/K	$\rho_w c_w t_w \pi r_1^2$
C_{w2}	4.98 J/K	$\rho_w c_w t_w \pi\left(r_2^2 - r_1^2\right)$

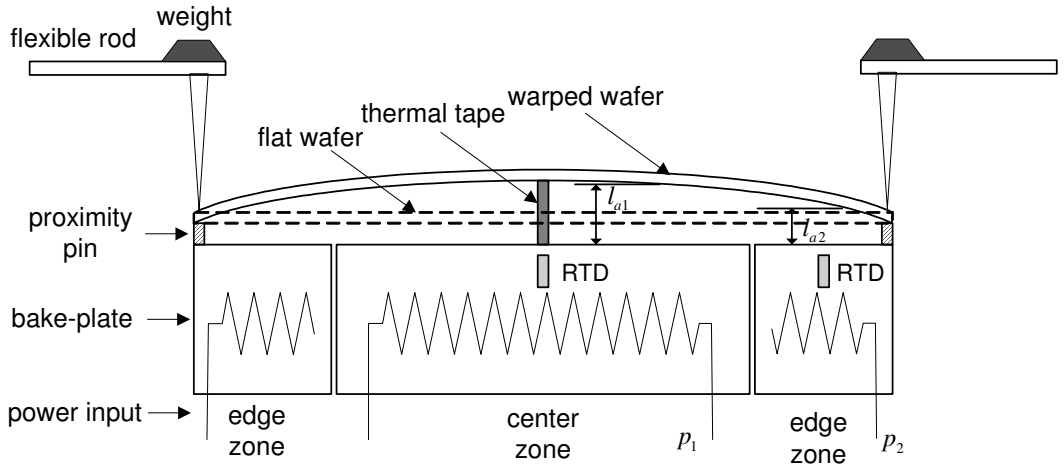


Fig. 2.3. Baking of Wafer.

A control software system was developed using the National Instruments LabView programming environment (http://www.ni.com, 2007). Two proportional-integral controllers of the following form were used to control the two zones of the bake plate.

$$u_1(t) = K_{c1}\left(e_1(t) + \frac{1}{T_{I1}}\int e_1(t)dt\right) \tag{2.5}$$

$$u_2(t) = K_{c2}\left(e_2(t) + \frac{1}{T_{I2}}\int e_2(t)dt\right) \tag{2.6}$$

$$e_1(t) = T_{p1}(\infty) - T_{p1}(t)$$

$$e_2(t) = T_{p2}(\infty) - T_{p2}(t)$$

where $u_1(t)$, $u_2(t)$ are the control powers and $T_{p1}(\infty)$, $T_{p2}(\infty)$ are the bake plate temperature setpoints. The proportional-integral controller parameters for the center and edge zones were manually tuned (Franklin *et al.*, 2002) as $K_{c1} = 5.15$, $T_{I1} = 150$ and $K_{c2} = 16.79$, $T_{I2} = 500$ respectively.

The relationship between the steady-state wafer temperatures $T_{w1}(\infty)$, $T_{w2}(\infty)$ and bake plate setpoints, $T_{p1}(\infty)$, $T_{p2}(\infty)$ for the two-zone system can be obtained

from Equations (2.1) and (2.2) as

$$T_{p1}(\infty) = R_{a1}\left(\frac{1}{R_{T1}}T_{w1}(\infty) - \frac{1}{R_{w12}}T_{w2}(\infty)\right) \quad (2.7)$$

$$T_{p2}(\infty) = R_{a2}\left(\frac{1}{R_{T2}}T_{w2}(\infty) - \frac{1}{R_{w12}}T_{w1}(\infty)\right) \quad (2.8)$$

where

$$R_{T1} = \frac{R_{w1}R_{a1}R_{w12}}{R_{a1}R_{w12} + R_{w1}R_{w12} + R_{w1}R_{a1}}$$

$$R_{T2} = \frac{R_{w2}R_{a2}R_{w12}}{R_{a2}R_{w12} + R_{w2}R_{w12} + R_{w2}R_{a2}}$$

2.3 Experiment

2.3.1 Setup

In all the experiments, commercial chemical amplified resist, Shipley UV3 was spin-coated at 6000 revolutions per minute on a 4-inch wafer. After a post-apply bake, the wafer went through an exposure tool with a patterned mask of regularly spaced lines. The exposed photoresist was then baked, developed and the final output was the linewidth of the photoresist pattern or CD. CD was measured with the scanning electron microscope (SEM). The value was taken as the average of 3 points. Except for the real-time on-line adjustment of the post-exposure bake temperature, all other inputs to the photolithography processes such as spin speed, baking time, exposure dose, develop time etc. were kept constant. No anti-reflection coating was used. The post-exposure bake time was fixed at 90s.

The experimental setup for the post-exposure bake of a warped wafer is shown in Figure 2.3. A fixed warpage was ensured during the baking experiment by

mechanically pressing the edges of the wafer against the proximity pins of 70μm. The center-to-edge warpage was given by the difference between the height of proximity pin and thermal tape thickness.

2.3.2 Runs

Twelve Experiment (Wafer) Runs were performed. On each wafer CD were monitored at 2 points, 1.5 inches apart, one near the center, the other near the edge of the wafer. At each point, three samples of linewidths were measured by scanning electron microscope to give the average CD in Figure 2.4. The results for Runs 1, 4, 7, 10 are tabulated in Table 2.3 for further discussion. The other runs were repeat experiments. Wafers 1–3 and 7–9 were flat while 4–6 and 10–12 were warped 140μm center-to-edge.

Because photoresist was coated on the patterned wafer, it was not convenient to attach temperature sensors on the wafer to measure wafer temperature. To do so, another set of experiments with the same wafer warpage and bake plate setpoints were conducted. There were no pattern nor photoresist on these wafers and their sole purpose was for us to obtain the wafer temperatures. Resistance Temperature Detectors (RTD) were attached to the wafers (El-Awady *et al.*, 2004; Tay *et al.*, 2004*a*) for temperature measurements. Thermal grease was applied to the RTD sensors for better heat transfer. The measured wafer temperatures are included in the last row of Table 2.3 and in the column that corresponded to the warpage and bake plate setpoints. Figure 2.5 shows the measured wafer temperature for a

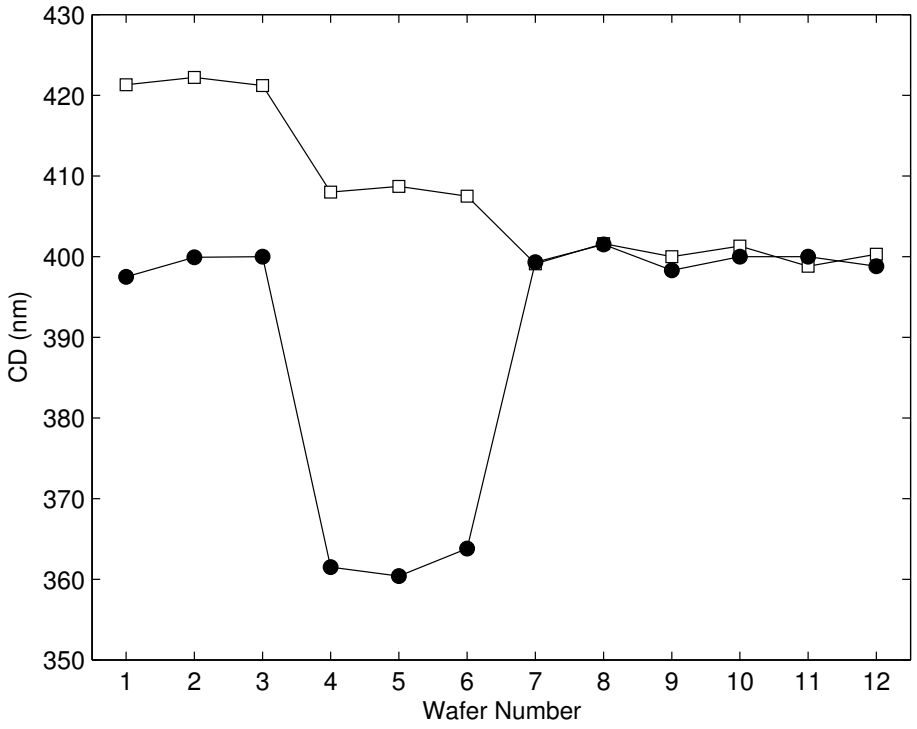


Fig. 2.4. Critical dimension measurements. Circle: center; Square: edge. Wafer 1–3: flat wafer with conventional baking; Wafer 4–6: warped wafer with conventional baking; Wafer 7–9: flat wafer with optimized baking; Wafer 10–12: warped wafer with real-time on-line adjustment of bake plate temperature setpoints.

warped wafer. The wafer was baked for 90s starting from $t = 10$s.

The bake plate temperature curve for Flat Wafer 1 is shown in Figure 2.1. Notice in Table 2.3 that for Flat Wafer 1 even though the wafer temperature at center (128.1°C) and edge (128.0°C) were approximately equal, CD nonuniformity was 23nm. This can be expected as properties at center and edge may not be the same e.g. the thickness of the coat of photoresist across the wafer is known to be nonuniform (Lee *et al.*, 2002; Decre and Vromans, 2000). Nonuniform photoresist thickness can cause nonuniform CD through a swing curve effect (Singh *et al.*, 2006; Yu *et al.*, 2005*a*; Yu *et al.*, 2005*b*). In Tay *et al.* (2007*a*) the bake plate

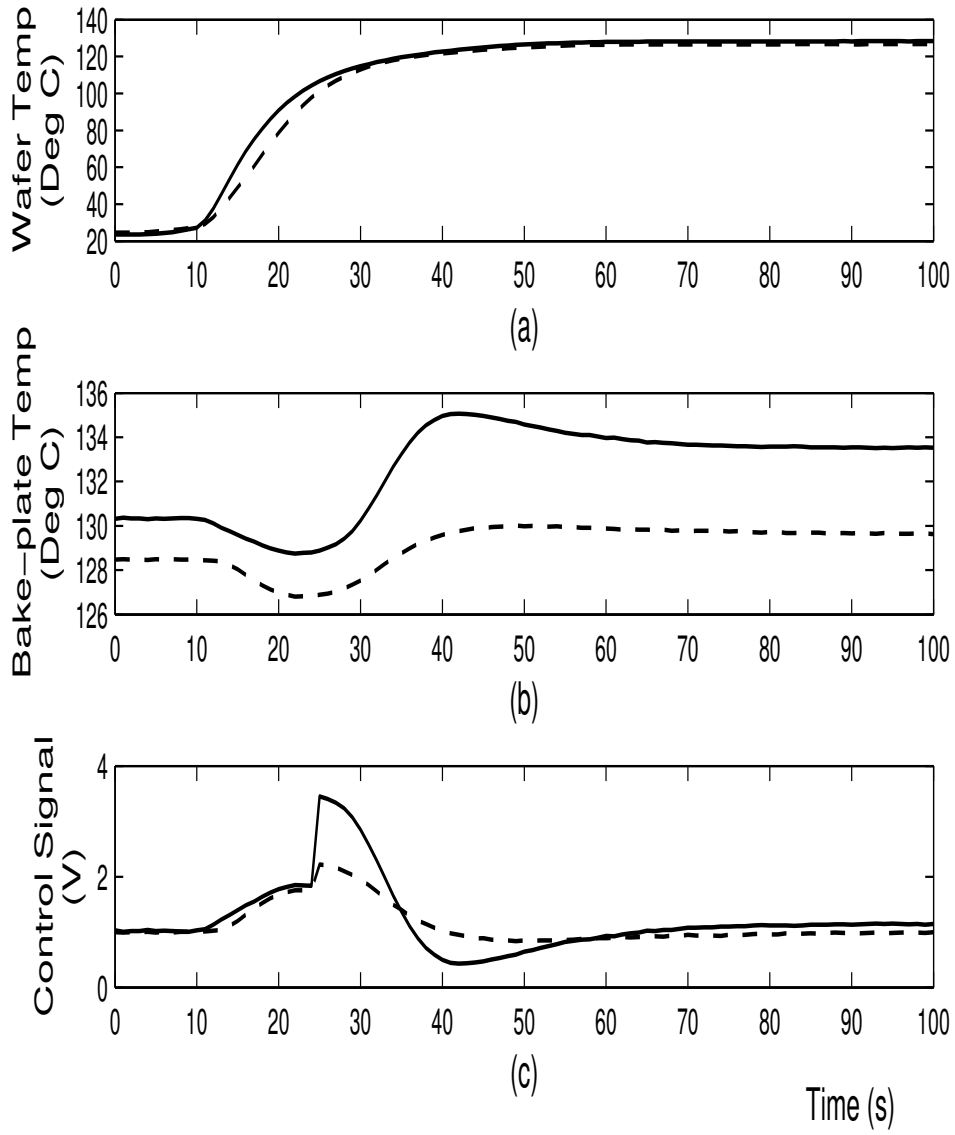


Fig. 2.5. Temperature measurement on a warped wafer with no photoresist nor pattern. Solid-line: center; Dashed-line: edge. The first plot shows the wafer temperature measured with RTDs. The second plot shows bake plate temperature where setpoint adjustments are made in the midway. The third plot shows the control signal.

Table 2.3. Experimental Results

Experiment (Wafer) No.		1	4	7	10
Warpage		Flat	Warp	Flat	Warp
Bake plate Setpoint (°C)	Center	130	130	130.3	130.3 to 133.6
$T_p(\infty) + T_a^*$	Edge	130	130	128.5	128.5 to 129.6
Bake plate Maximum	Center	2.13	1.54	2.12	1.54
Temperature Drop (°C)	Edge	1.98	1.73	1.98	1.70
CD (nm)	Center	399	362	399	399
	Edge	422	408	400	400
	Nonuniformity†	23	46	1	1
Wafer Temperature (°C)	Center	128.1	125.4	128.2	128.2
$T_w(\infty) + T_a^*$	Edge	128.0	126.9	126.6	126.6

*Ambient temperature $T_a = 24.5$°C.
†Difference between center and edge CD.

temperatures were controlled to give uniform temperatures on the wafer. It is demonstrated here that this is not good enough to give uniform CD. Nonuniform temperature distribution across the wafer may be required to obtain uniform CD at center and edge.

The bake plate temperature curve for Warped Wafer 4 is shown in Figure 2.2. Table 2.3 shows that the wafer center temperature (125.4°C) was lower than edge (126.9°C) and the CD nonuniformity doubled to 46 nm.

The manufacturing process should be fairly repeatable. In practice a certain degree of repeatability of the CD profile is expected and hence the two-zone bake plate should start baking at different temperatures for different zones. The desired CD profile is 400nm for the center and edge respectively. The desired wafer temperature profile to achieve uniform CD can be obtained from wafer 1-3 results

and the CD temperature sensitivity. Desired bake plate temperature profile for flat wafer can be obtained from Equations (2.7) and (2.8). Once a new set of bake plate setpoints (130.3°C and 128.5°C) was implemented as shown in Figure 2.6, the CD non-uniformity on the Flat Wafer 7 was reduced to 1 nm as shown in Table 2.3. Notice that for CD uniformity, wafer temperature at center (128.2°C) was higher than edge (126.6°C).

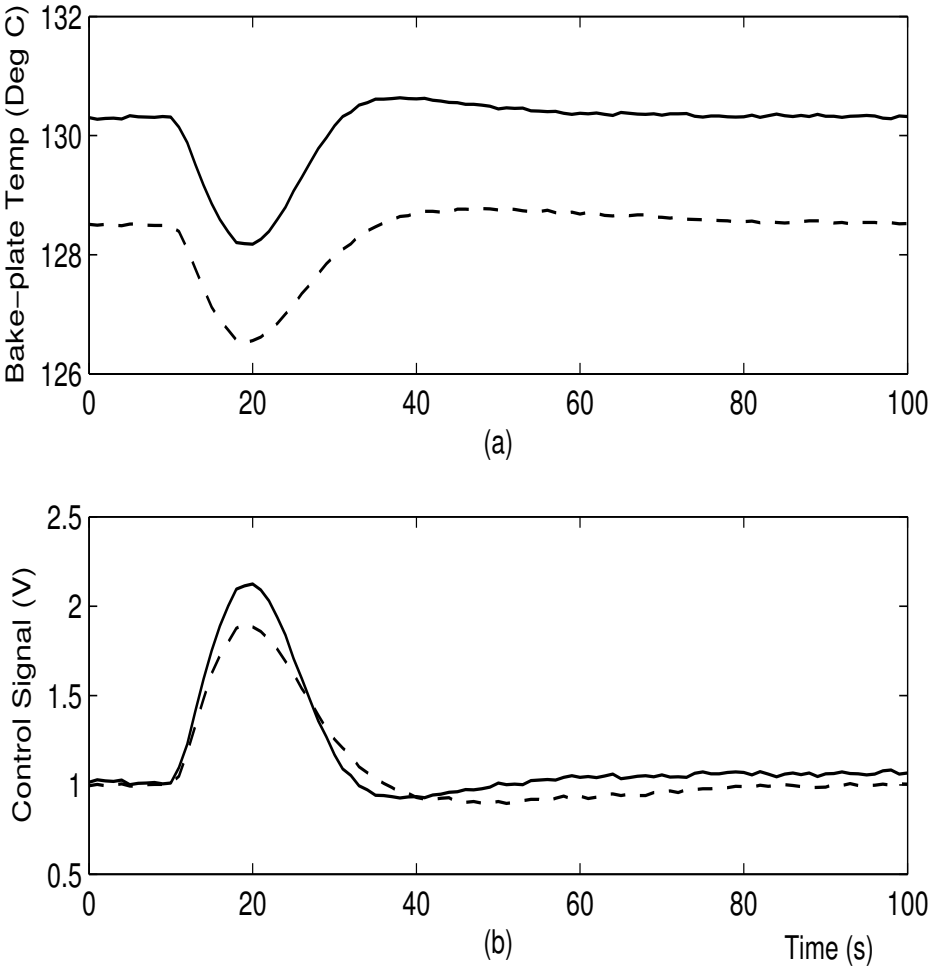


Fig. 2.6. Bake plate setpoint adjusted to give uniform CD for Flat Wafer 7. Solid-line: center; Dashed-line: edge.

2.3.3 Real-Time Control

For the given bake plate, all parameters in Table 2.2 are known except for R_{a1} and R_{a2} which depended on wafer warpage or average air-gaps at center-zone (l_{a1}) and edge-zone (l_{a2}). The center and edge zones were pre-programmed to start baking at setpoints of 130.3°C and 128.5°C respectively to give desired wafer temperatures of $T_{w1}(\infty) + T_a = 128.2$°C and $T_{w2}(\infty) + T_a = 126.6$°C and CD uniformity for flat wafers. Equations (2.1) to (2.6) were solved to determine the maximum temperature drops in T_{p1} and T_{p2} for $20\mu\text{m} \leq l_{a1} \leq 300\mu\text{m}$ and $20\mu\text{m} \leq l_{a2} \leq 300\mu\text{m}$ and the results are plotted in Figures 2.7 and 2.8 for l_{a1} and l_{a2} respectively. They can also be tabulated to facilitate on-line search for l_{a1} and l_{a2} from the maximum temperature drops.

To obtain CD uniformity for a warped wafer, setpoint adjustments were made in real-time once warpage was detected. Warpage differed from wafer to wafer and hence not expected to be repeatable. If warpage was repeatable then fixed but different bake plate setpoints could have been used for center and edge.

For processing of Warp Wafer 10, the maximum temperature drop of 1.54°C and 1.70°C center and edge respectively were first measured. A search through Figures 2.7 and 2.8 gave $l_{a1} = 184\mu\text{m}$ and $l_{a2} = 110\mu\text{m}$. Substitute into R_{a1}, R_{a2} and with the desired wafer temperatures of $T_{w1}(\infty) + T_a = 128.2$°C and $T_{w2}(\infty) + T_a = 126.6$°C, Equations (2.7) to (2.8) gave the new setpoints of $T_{p1}(\infty) + T_a = 133.6$°C and $T_{p2}(\infty) + T_a = 129.6$°C. Notice in Figure 2.9 the bake plate setpoints were changed from 130°C to 133.6°C and 128.5°C to 129.6°C at $t = 24$s,

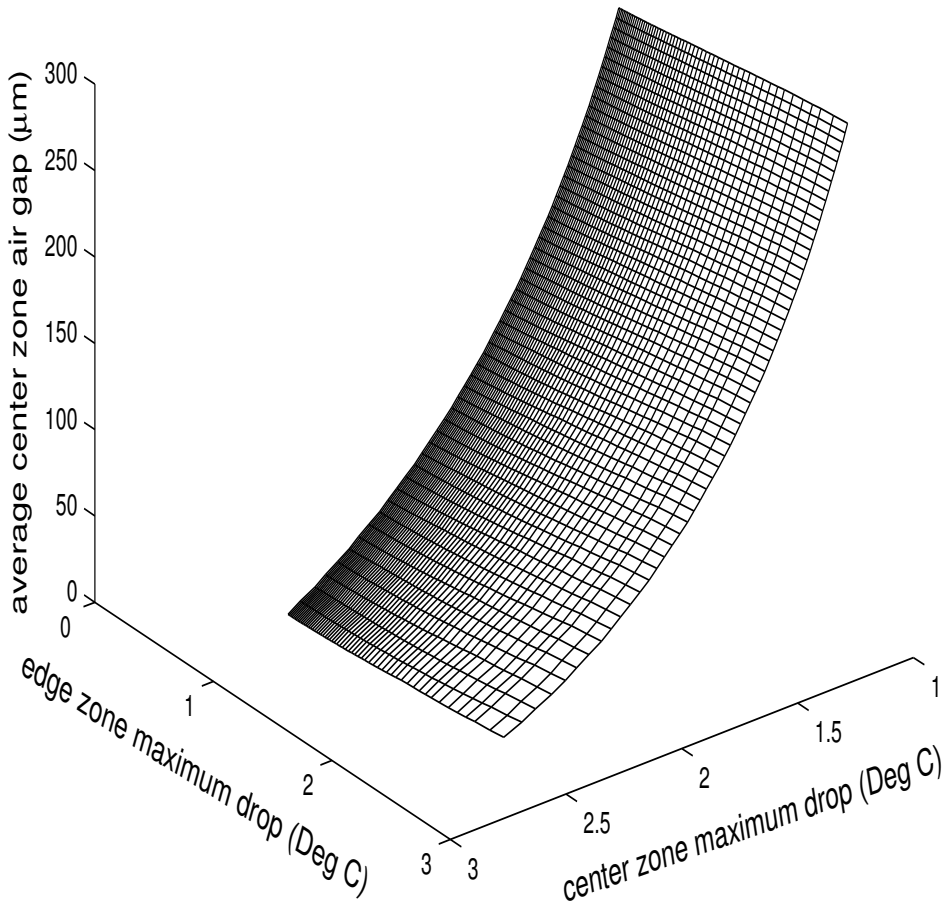


Fig. 2.7. Center-zone average air-gap versus bake plate maximum temperature drops.

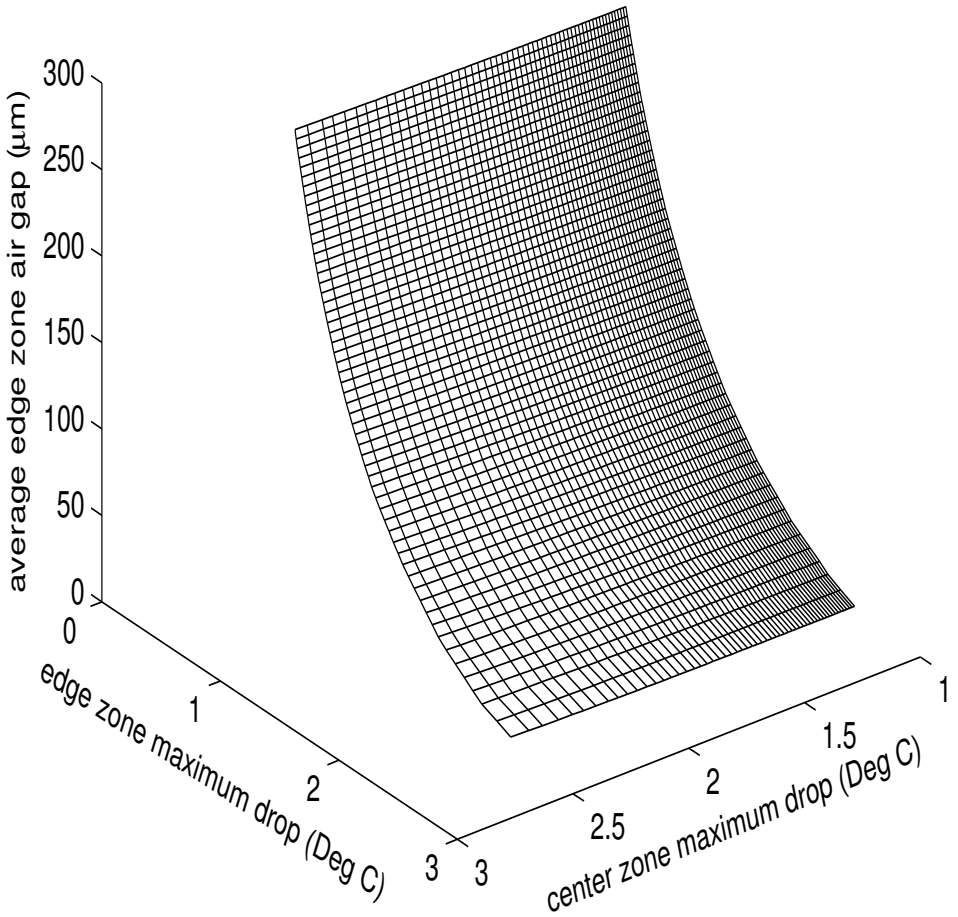


Fig. 2.8. Edge-zone average air-gap versus bake plate maximum temperature drops.

immediately after the maximum bake plate temperature drops had occurred. CD non-uniformity of 1 nm and wafer temperatures of 128.2°C (center) and 126.6°C (edge) were obtained, just like Flat Wafer 7.

Note that $l_{a1} - l_{a2} = 74\mu\text{m} \neq 140\mu\text{m}$ the center-to-edge warpage of Wafer 10 because l_{a1} and l_{a2} were not the air-gaps at the wafer center and extreme edge but the average over the center-zone and edge-zone. Based on the estimated air-gap l_{a1}, l_{a2} and together with the proximity pin height, the profile of the wafer can be obtained by extrapolation as shown in Figure 2.10. An estimated warpage of 148μm from center to edge for the warped wafer is obtained which is close to the known warpage of 140μm.

2.4 Application for One-Zone Bake Plate

In semiconductor industry one-zone bake plate are still widely used for baking in lithography (Do *et al.*, 2004). For applications on one-zone bake plates, the above strategy can be simplified to a single-input-single-output problem.

Experiments were carried on a one-zone bake plate, as shown in Figure 1.2. Quartz mask was used with pattern as regularly spaced lines. Shipley SL4000 photoresist was used. Six wafer runs were conducted and the temperature readings and SEM CD measurements are tabulated in Table 2.4. The CD value was taken as the average of 5 points. Wafer 1 was flat, 2 and 3 were of known warpage and the temperature curves are shown in Figure 1.3 as solid-line, dashed-line and dashed-dotted-line respectively. Conventional baking was performed for warped wafer 2,

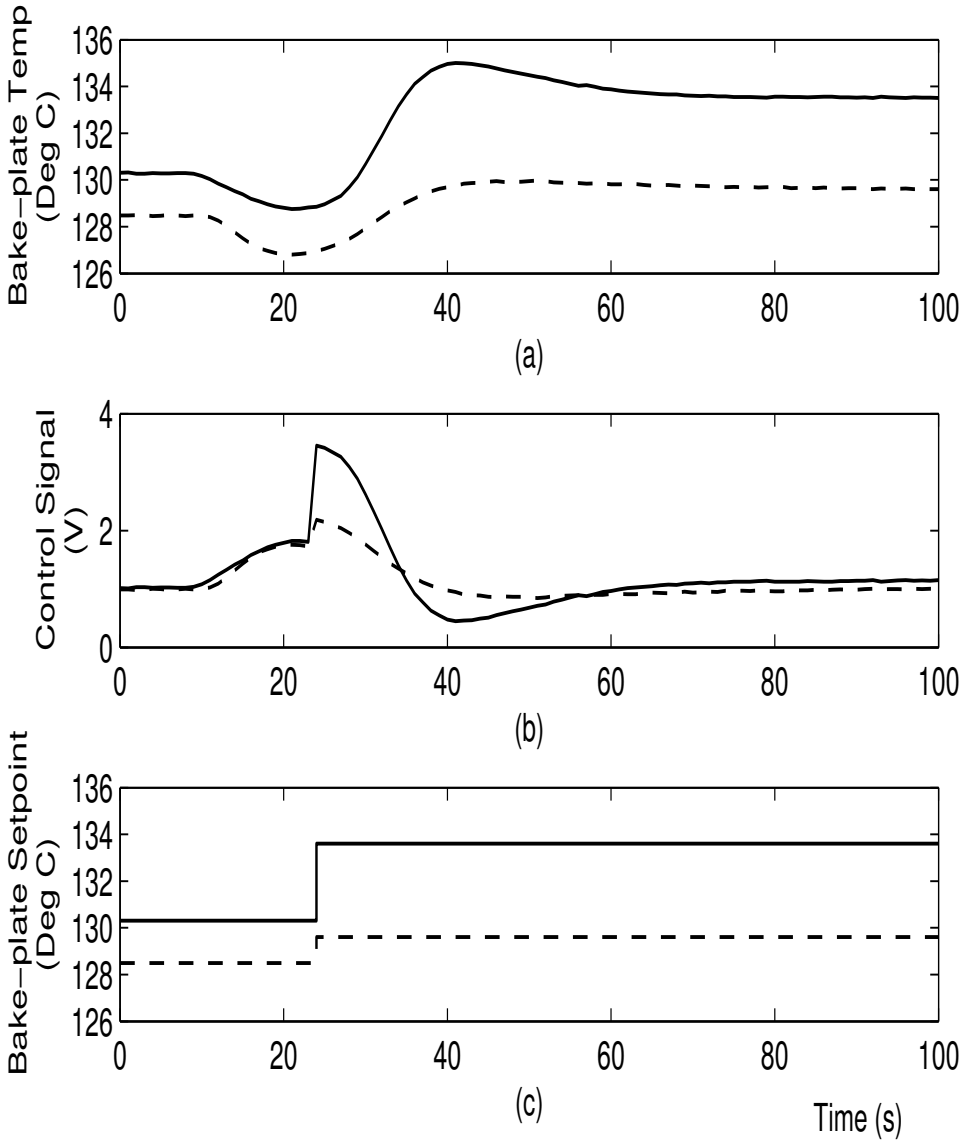


Fig. 2.9. Bake plate setpoints adjusted in real-time once warpage was detected to give uniform CD for Warped Wafer 10. Solid-line: center; Dashed-line: edge.

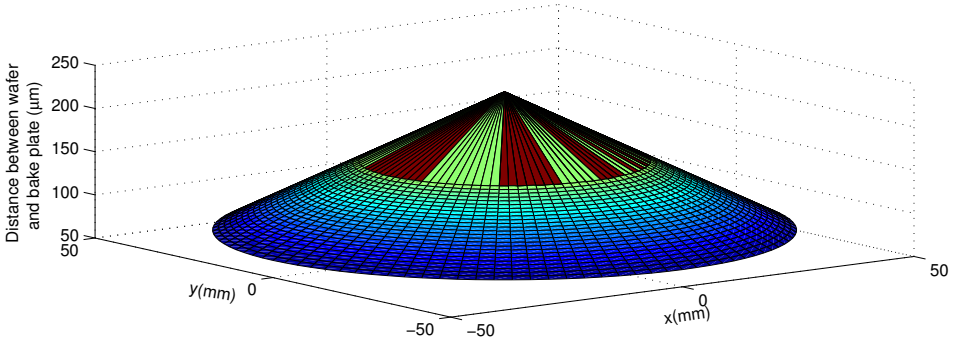


Fig. 2.10. Estimated profile of warped wafer 10

and real-time temperature control strategy was performed for warped wafer 3. The nominal air-gap can be determined from Figure 2.12, as given in Table 2.4 Column (e). Based on the estimated air-gap and together with the proximity pin height, the profile of the warped wafer 3 can be obtained by extrapolation as shown in Figure 2.11.

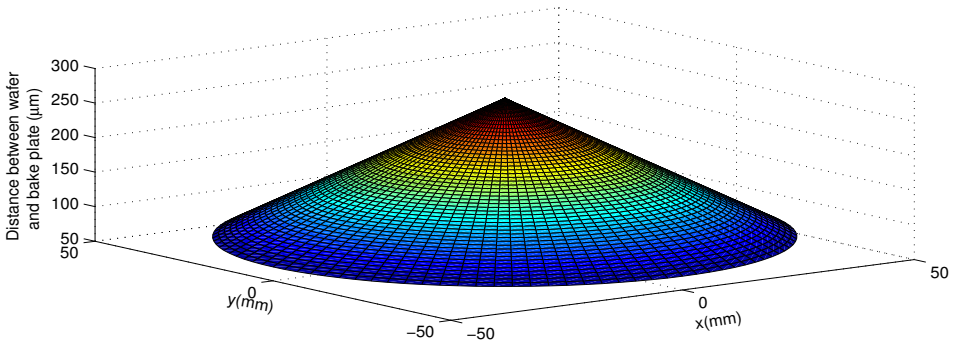


Fig. 2.11. Estimated profile of warped wafer 3

The experimental runs and results for Wafers 4, 5 and 6 in Table 2.4 were similar to Wafers 1, 2 and 3 respectively, demonstrating repeatability. Experimental results showed that for a wafer warped 140μm center-to-edge, the CD variation was over 20nm. With real-time temperature control strategy, however, the CD

nonuniformity between flat wafer and warped wafer was reduced to around 2nm. On average the improvement is 10 times.

In the multizone application, different zones of the bake plate can be adjusted to different temperature to improve within-wafer CD uniformity. Because of the lack of such capability, one-zone bake plate can't achieve good within-wafer CD uniformity.

Table 2.4. Experimental Results ($T_a = 24°C$)

(a) Wafer No.	(b) Flat or Warp Wafer	(c) Minimum Bake Plate Temp. (°C)	(d) Maximum Temp. Drop (°C)	(e) l_a Average Air-Gap (μm)	(f) $T_w(\infty) + T_a$ Wafer Temp. (°C)	(g) $T_p(\infty) + T_a$ Bake Plate Temp. (°C)	(h) CD (nm)
1	Flat	103.15	1.85	70	103.5	105.0	341.8
2	Warp	103.58	1.42	170	101.5	105.0	321.3
3	Warp	103.58	1.42	170	103.5	107.1	341.0
4	Flat	103.13	1.87	65	103.6	105.0	342.7
5	Warp	103.57	1.43	166	101.6	105.0	322.3
6	Warp	103.61	1.39	177	103.5	107.2	340.4

2.5 Conclusion

The experimental results on CD control for a warped wafer are presented. To obtain CD uniformity for a warped wafer, bake plate setpoints adjustments were made in real-time and on-line once warpage was detected and this could result in nonuniform temperature distribution across the wafer. For wafers warped 140μm center-to-edge, CD nonuniformity was reduced to 2 nm.

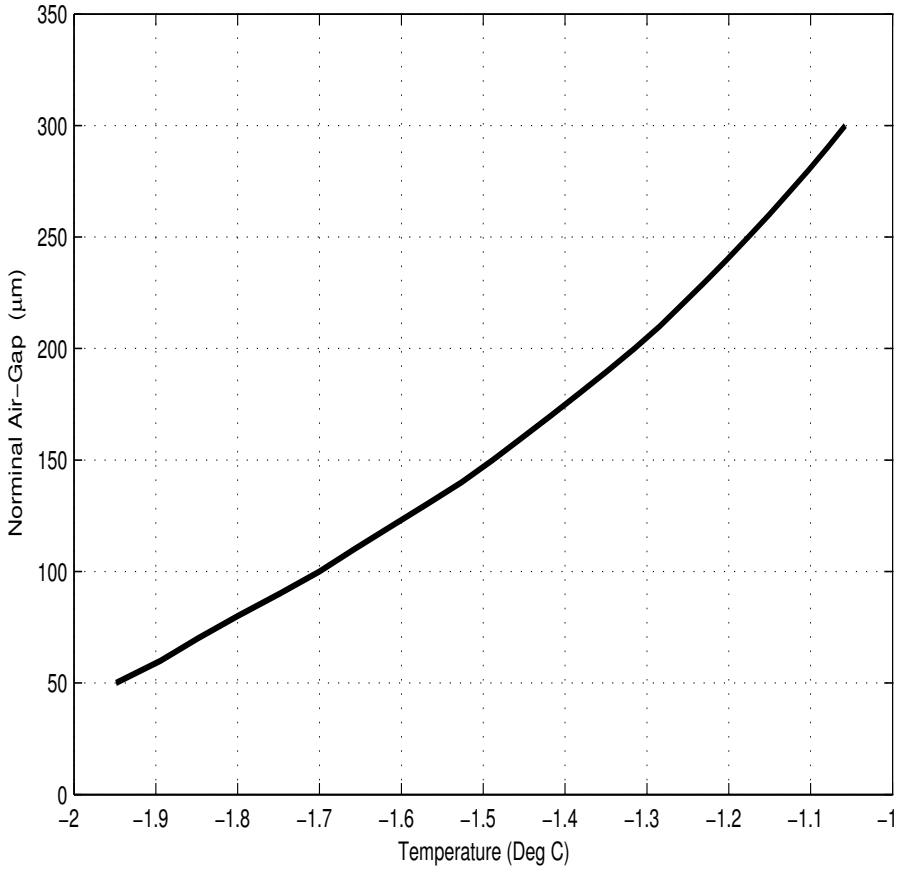


Fig. 2.12. Nominal air-gap, l_a, versus maximum temperature drop.

Chapter 3

CD Uniformity via Real-Time Photoresist Thickness Control

This Chapter describes the experimental results on wafer-to-wafer and within-wafer Critical Dimension (CD) control. It is known that photoresist thickness affects CD. In this Chapter, photoresist thickness is controlled to improve CD uniformity. As opposed to run-to-run control where information from the previous wafer or batch is used for control of the current wafer or batch, the approach here is real-time and make use of the current wafer information for control of the current wafer CD. The experiments demonstrated that such an approach can reduce CD non-uniformity wafer-to-wafer and within-wafer.

3.1 Introduction

The key output in photolithography is the linewidth of the photoresist pattern or CD. The CD is significantly impacted by several variables that must also be monitored to ensure quality (Kim *et al.*, 2004). Improvements to CD uniformity have been made through optimization of various lithography sequences. They include die-to-die exposure dose optimization (Schoot *et al.*, 2002), focus control (Chemali *et al.*, 2004), grid size adjustment for optical proximity correction (Lee *et al.*, 2004*a*), writing a multitude of shading elements inside the mask to adjust wafer level CD uniformity (Morikawa *et al.*, 2006), post-exposure bake temperature profile optimization by adjusting heater power in a multizone controlled bake plate (Zhang *et al.*, 2005; Berger *et al.*, 2004*a*; Ruck *et al.*, 2007).

Photoresist thickness variation is one of the major contributors of CD variations (Berger *et al.*, 2006). Photoresist is typically spin coated on the wafer and its thickness and uniformity are controlled in part by the spin speed and ramp of spin coaters as well as the volatility of the solvent and the viscosity of the resist (May and Spanos, 2006; Kim *et al.*, 2002; Manu, 2003). The final thickness is also affected by environmental conditions. Photoresist thickness non-uniformity of $\pm 2\%$ were reported (Bagen *et al.*, 1996; Decre and Vromans, 2000). Non-uniform lithography properties are expected and they vary as a swing curve or sinusoidal function of photoresist thickness due to thin film interference effects. The swing curve effect for an alternating phase shift mask was studied by Singh *et al.* (2006). With the application of high numerical aperture exposure tools, the characteristic of swing

curve with high numerical aperture was given by Dio (2006), Bauer *et al.* (2006) and Brunner *et al.* (2002). An analytical study of resist CD variation with respect to resist thickness was carried out using rigorous electromagnetic theory (Yu *et al.*, 2005*a*; Yu *et al.*, 2005*b*).

With stringent specification on CD, the demand for a uniform and repeatable resist thickness can be expected. Besides improving the spin coating process itself, the next process after spin-coating, i.e., post-apply bake or softbake, can be optimized. By adjusting post-apply bake time, lithographic performance was enhanced for two negative chemically amplified resists (Raptis, 2001). During post-apply bake, residual solvent evaporates and leaves empty volume behind resulting in film thickness reduction (Tortai, 2004). For Shipley UV3, a theoretical model was developed and matched with experimental data (Hsu *et al.*, 2001).

Lee *et al.* (2002) demonstrated that within-wafer photoresist thickness non-uniformity can be reduced by manipulating post-apply bake temperature. For the proposed post-apply bake experiment to be useful, it should impact the CD output positively. In this Chapter, the effect of the post-apply bake experiment on wafer-to-wafer and within-wafer CD control is to be demonstrated. The approach here is real-time and make use of the current wafer information for control of the current wafer CD.

3.2 Experimental Setup

In the experiments, commercial chemically amplified resist, Shipley UV3 was spin-coated at 6000 revolutions per min on a 4-inch wafer. The wafer next went through an exposure tool with a patterned mask of regularly spaced lines. The exposed photoresist was then baked, developed and the final output was the linewidth of the photoresist pattern or CD. CD was measured with the scanning electron microscope. The value was taken as the average of 3 points. Except for the real-time on-line adjustment of the post-apply bake temperature, all other inputs to the photolithography processes such as spin speed, baking time, exposure dose, develop time etc. were kept constant. No anti-reflection coating was used.

The post-apply bake setup used to control resist thickness is shown in Figure 3.1. It consists of a bake plate, a thickness sensor, and a thickness controller. Figure 3.2 shows the photograph of the experimental setup with a 4-inch wafer sitting on top of the bake plate. A thickness sensor is mounted directly above the wafer to monitor the resist thickness.

3.2.1 Thickness Sensor

It comprises a broadband light source, a spectrometer with the capability of monitoring the reflected light intensity (SQ2000) at different wavelength and a bifurcated fiber optics reflection probe. The reflection probe consists of a bundle of 7 optical fibers (6 illumination fibers around 1 read fiber). During post-apply bake, light from the broadband light source is focused on the resist through one end of the

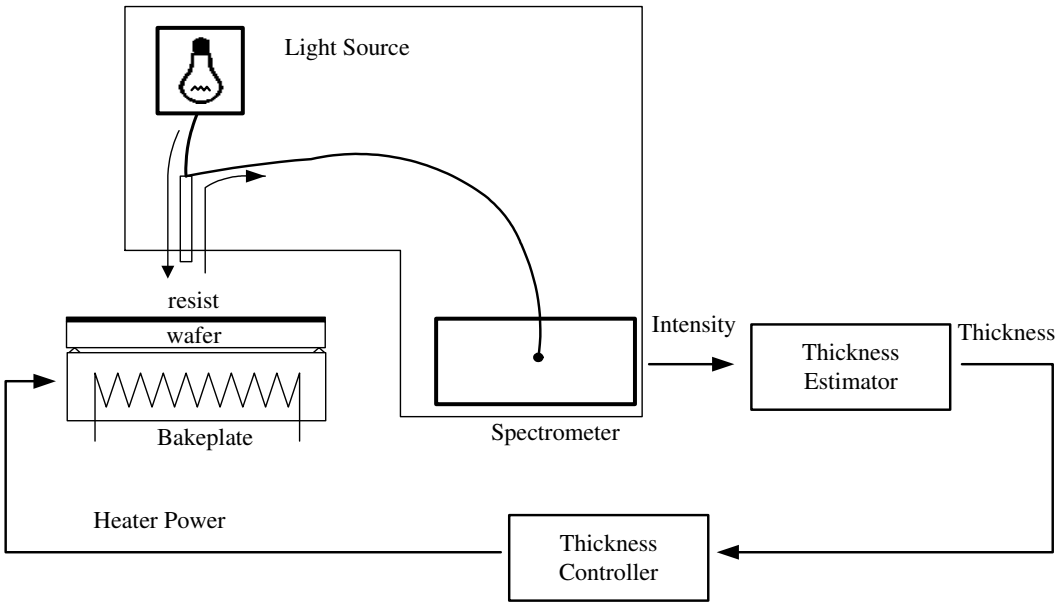


Fig. 3.1. Experimental Setup.

probe and the reflected light is guided back to the spectrometer through the other end. By measuring the reflected light intensity over a band of wavelength, the resist thickness can be monitored in real-time using least square estimation method. A filter was used to block out the shortwave light, preventing damage to the photosensitive resist. When light is focused onto the resist film, phase difference between the incident and reflected light creates interference effects within the resist. Resist thickness can be estimated from the reflectance signals of the multiwavelength spectrometer using a thin-film optical model. The spectrometer, enclosed by a frame in Figure 3.1, together with a thickness estimator are used for in-situ measurements of the resist thickness. With the incoming light at normal incidence, the observed reflectance signal h is given by (Vincent *et al.*, 1997; Fowles, 1989).

$$h(\lambda, y) = \left(\frac{r_1 e^{i\sigma} + r_2 e^{-i\sigma}}{r_1 r_2 e^{-i\sigma} + e^{i\sigma}} \right) \left(\frac{r_1 e^{i\sigma} + r_2 e^{-i\sigma}}{r_1 r_2 e^{-i\sigma} + e^{i\sigma}} \right)^* \tag{3.1}$$

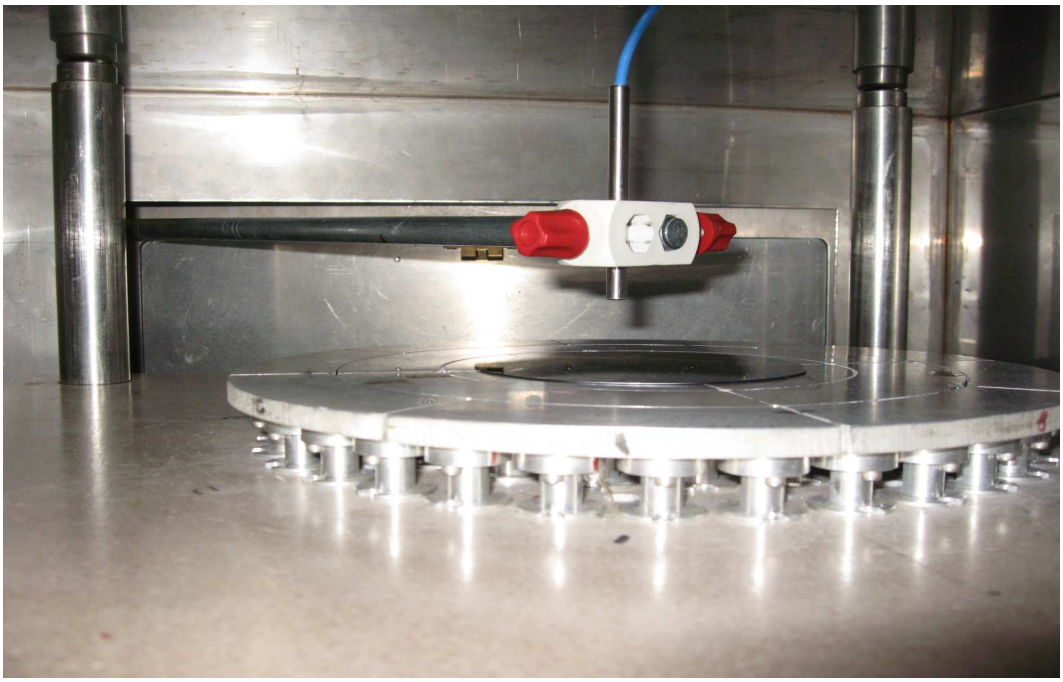


Fig. 3.2. Plant photo for the post-apply bake process.

where $r_1 = \frac{n_a - n_r}{n_a + n_r}$ $r_2 = \frac{n_r - n_s}{n_r + n_s}$ $\sigma = \frac{2\pi n_r y}{\lambda}$

n_a, n_r, n_s are the refractive index of air, resist, and substrate, respectively. The relation of the refractive index with wavelength is given by the Cauchy equation (Born and Wolf, 1999)

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4}$$

With the reflectance measurements from the spectrometer, the resist thickness can be estimated using 3.1. The solution to the problem is nonconvex and there is no global minimum over the search space. However, there is a reasonably good initial estimate of the resist thickness from the coating process. With known coating speed, the initial thickness can be estimated from the photoresist spin curve which is usually provided in the product data sheet. Therefore, a local minimum solution for the resist thickness can be obtained using least squares estimation. To realize

this, equation 3.1 is approximated with the Taylor series expansion

$$h(\lambda, y) = h(\lambda, y_0) + \left.\frac{\partial h}{\partial y}\right|_{\lambda, y_0} \triangle y \tag{3.2}$$

where y_0 is the initial thickness estimation. The estimated resist thickness $\hat{y}$ is given as

$$\hat{y} = y_0 + \triangle y$$

and the change in thickness $\triangle y$ is given using least square estimation as

$$\triangle y = \left(\frac{\partial h^T}{\partial y}\frac{\partial h}{\partial y}\right)^{-1}\frac{\partial h^T}{\partial y}(h - h_0)$$

where

$$\frac{\partial h}{\partial y} = \begin{bmatrix} \left.\frac{\partial h}{\partial y}\right|_{\lambda_1, y_0} \\ \left.\frac{\partial h}{\partial y}\right|_{\lambda_2, y_0} \\ \vdots \\ \left.\frac{\partial h}{\partial y}\right|_{\lambda_M, y_0} \end{bmatrix} \qquad h = \begin{bmatrix} h(\lambda_1, y) \\ h(\lambda_2, y) \\ \vdots \\ h(\lambda_M, y) \end{bmatrix} \qquad h_0 = \begin{bmatrix} h(\lambda_1, y_0) \\ h(\lambda_2, y_0) \\ \vdots \\ h(\lambda_M, y_0) \end{bmatrix}$$

M is number of reflectance measurements among the spectrometer wavelength range. The sampling interval is 1s. The first initial thickness estimate y_0 can be obtained from the spin-coating process thickness estimation. Later on, the initial y_0 will be updated with current $\hat{y}$.

There are two other estimation methods: nonlinear estimation and fringe counting. The nonlinear estimation method uses equation 3.1 to search for a solution. It gives the most accurate measurements since no approximation is made to equation 3.1. However, it takes a long estimation time. The fringe counting method simply uses the distance between the peaks and valleys in the reflectance signals

to estimate the resist film thickness. This method take less estimation time, but it is less accurate at the same time. A one-order Taylor approximation is carried on for the least square estimation method to reduce the estimation time dramatically. Further more, the error between least square estimation and nonlinear estimation can be fairly neglected (Lee *et al.*, 2002). Thus the least square method is most suitable for real-time application.

3.2.2 Thickness Controller

The commonly used controller is the proportional-integral (PI) controller (Ho *et al.*, 2000) as shown in Figure 3.3 and given as

$$\begin{aligned} u(t) &= K_C \left(e(t) + \frac{1}{T_I} \int e(t)dt \right) \\ e(t) &= y_r(t) - y(t) \end{aligned} \tag{3.3}$$

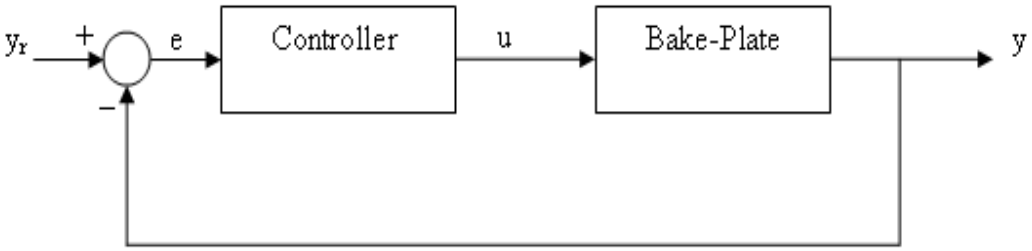


Fig. 3.3. Block diagram of the control system.

where $u(t)$ is the control voltage. In the standard temperature control implementation, $y(t)$ and $y_r(t)$ are the measured and desired bake plate temperature respectively. In this implementation, $y(t)$ and $y_r(t)$ are the measured and desired photoresist thickness respectively. K_C and T_I are the controller gains.

3.3 Experimental Results

As shown in Figure 3.4, with the availability of the thickness measurements (solid-line), the PI controller computed the heater power to follow a pre-defined desired resist thickness profile (dotted-line). If the photoresist was thicker (thinner) than the desired profile the controller would increase (decrease) the baking temperature such that the photoresist thickness converged to the desired profile.

3.3.1 Wafer-to-Wafer CD Control

In semiconductor manufacturing, categories for subgroups monitoring include wafer-to-wafer and within-wafer variations (May and Spanos, 2006). CD uniformity wafer-to-wafer will be discussed here and within-wafer in the next section. Nine wafer runs are shown in Figure 3.5. Photoresist and CD at a point one inch from the center of the wafer were monitored. The average linewidth or CD and the photoresist thickness at the end of the 90 seconds post-apply bake are plotted in Figures 3.5a and 3.5b respectively. For Wafers 1 to 4, the photoresist thickness were controlled during post-apply bake and photoresist thickness deviation and CD deviation of 1 nm and 2 nm respectively were obtained wafer-to-wafer. In contrast, photoresist thickness were not controlled during post-apply bake for Wafers 5 to 9 and larger deviations were obtained.

The baking experiment for Wafer 1 is given by the solid-line in Figure 3.4. The proportional-integral controller parameters K_C and T_I were manually set as 0.08 and 1000 respectively. Notice that the controller raised the baking temperature

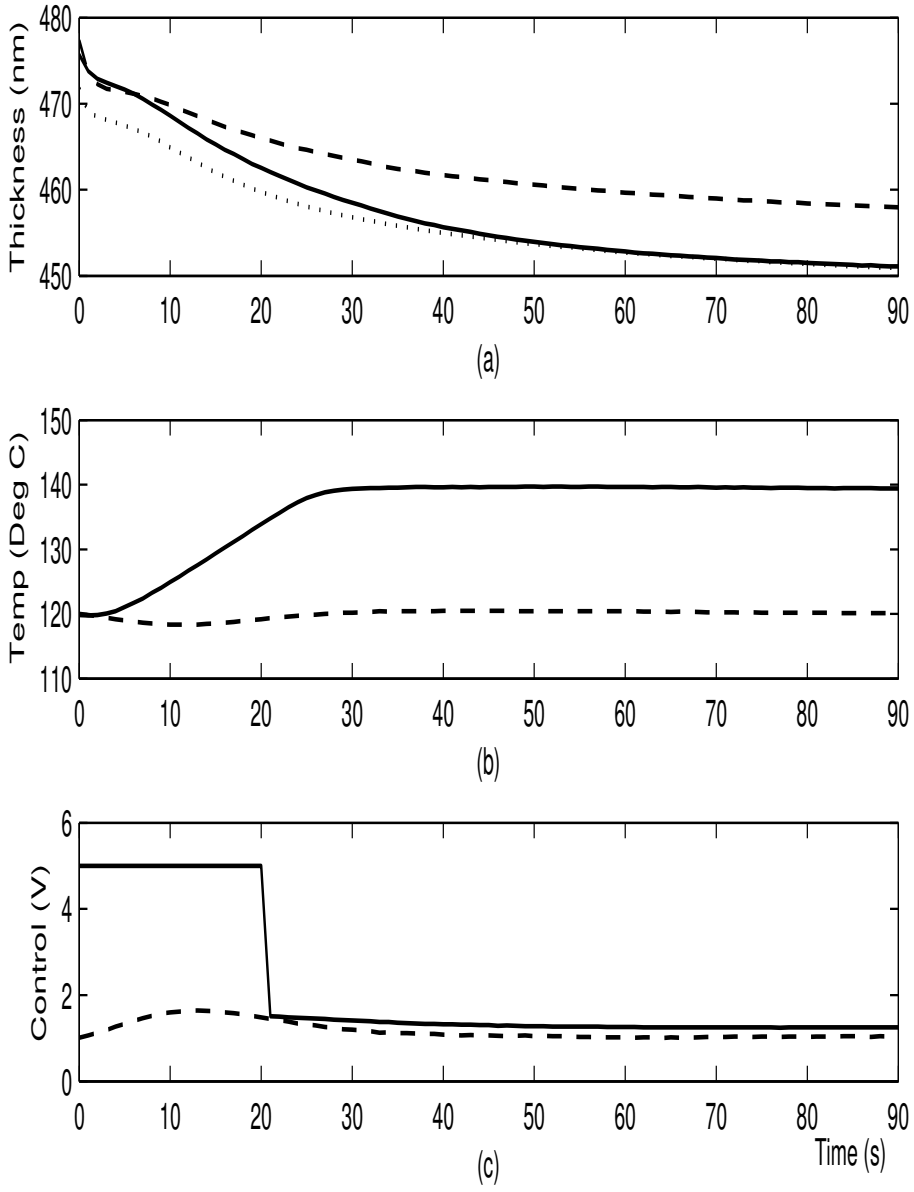


Fig. 3.4. Post-apply bake. (a) Photoresist thickness. (b) Bake plate temperature. (c) Control signal, u, in Voltage (V). Solid-line: Wafer 1; dashed-line: Wafer 5; dotted-line: desired photoresist thickness.

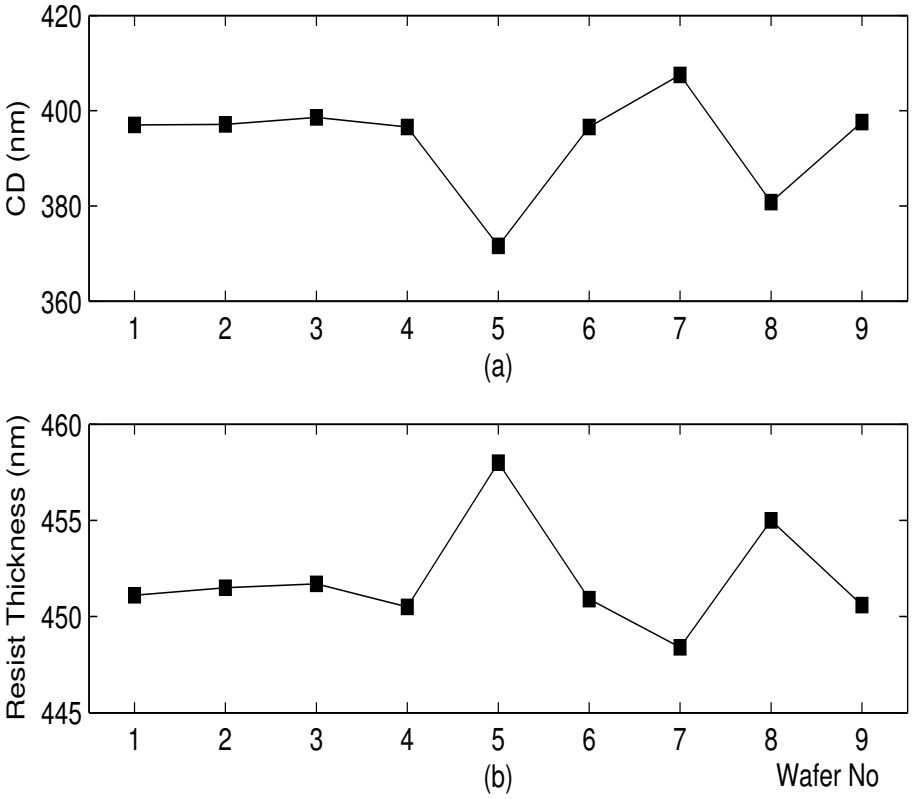


Fig. 3.5. Wafer-to-Wafer photoresist thickness and CD.

from 120°C to 140°C to reduce the photoresist thickness to the desired thickness (dotted-line). The average photoresist thickness should be chosen as the desired thickness. If not, to bring "faraway" thickness to the desired thickness could result in very high or low temperatures causing other problems such as decomposition of the photoactive compound of the resist if temperature was too high. If the average photoresist thickness was chosen as the desired thickness then as shown in Figure 3.5, Wafers 6 and 9 were at the desired thickness even though no thickness control or corrective action were performed during post-apply bake and their CD were also equal to the CD of Wafers 1 to 4.

The baking experiment for Wafer 5 is given by the dashed-line in Figure 3.4.

Since photoresist thickness control was not implemented during post-apply bake, the photoresist thickness did not converge to the desired thickness profile. In this case, standard temperature control was implemented where the desired temperature, $y_r(t)$, was fixed at 120°C. A number of these standard temperature control experiments could be performed earlier. The photoresist profiles obtained could be averaged and then used as the desired thickness for the thickness control experiments.

3.3.2 Within-Wafer CD Control

Eight wafer runs are shown in Figure 3.6. On each wafer photoresist thickness was monitored at 2 points, 1.5 inches apart, one near the center, the other near the edge of the wafer. The proportional-integral controller parameters K_c, T_I were manually tuned (Franklin *et al.*, 2002) as 0.08, 1000 for the center and 0.02, 200 for the edge. Photoresist thickness uniformity control during post-apply bake was performed for Wafers 10 to 13 and the differences between the circles and squares in Figure 3.6 showed that the photoresist thickness deviations and CD deviations between the 2 points were about 1 nm and 2 nm respectively. Photoresist thickness uniformity control were not performed for Wafers 14 to 17 and the deviations were much larger.

The experiments were repeated as shown in Figure 3.7 for CD of 500nm. Photoresist thickness uniformity control were performed for Wafers 18 to 21 but not for Wafers 22 to 25.

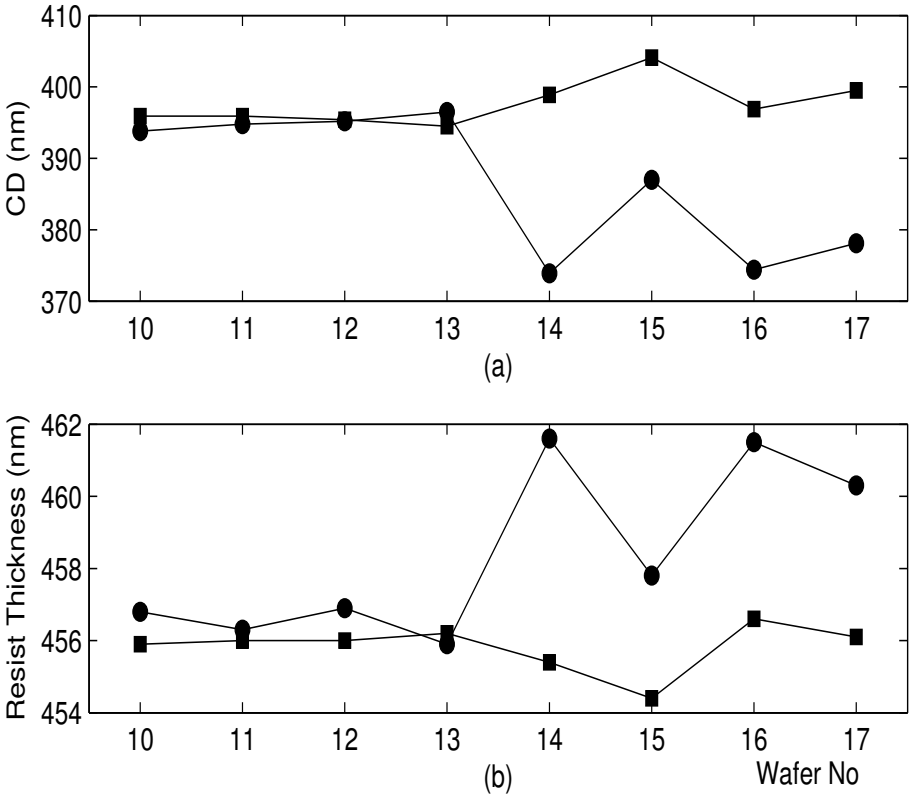


Fig. 3.6. Within-Wafer photoresist thickness and CD. Circle: near center of wafer; square: near edge of wafer.

Figure 3.8 shows the temperature and photoresist thickness profiles of the 2 points on Wafer 10. Notice that at the beginning of the post-apply bake process (time = 0) the photoresist thickness were different but converged to the desired thickness at the end. Notice also that the baking temperature was higher for the thicker resist (solid-line). As in the wafer-to-wafer case, the desired thickness was chosen such that it did not result in temperatures that were too high or too low. For this experiment, 2 probes were used instead of the 1 probe shown in Figure 3.2. The distributed thermal processing system used in this work (Tay *et al.*, 2007*a*) consisted of two heating zones, centre and edge as shown in Figure 3.9. Embedded

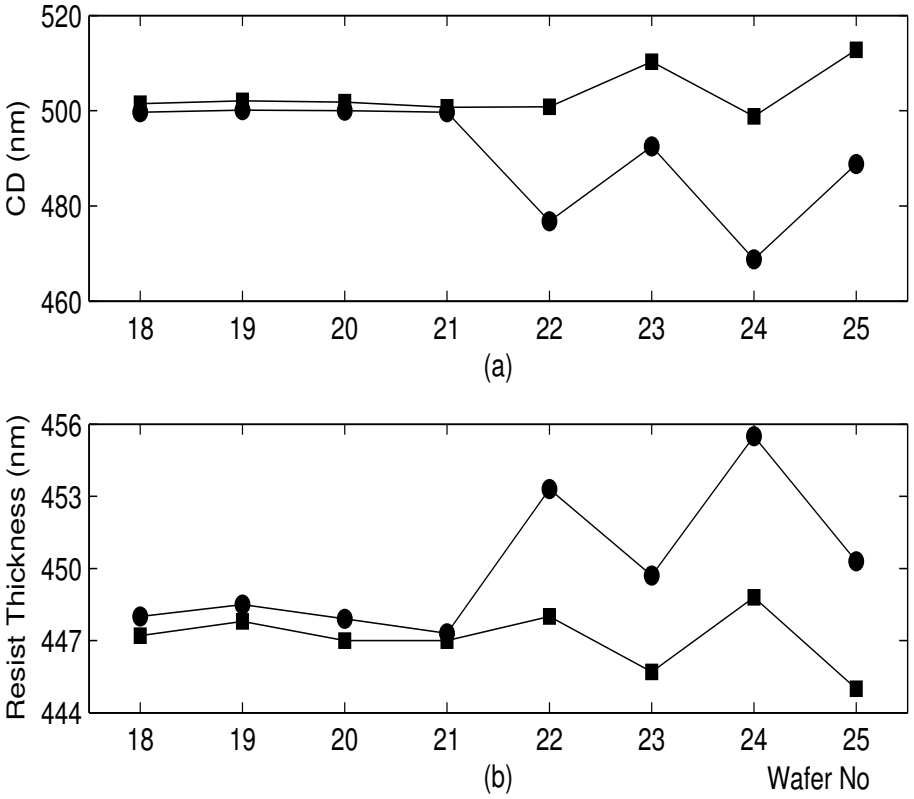


Fig. 3.7. Within-Wafer photoresist thickness and CD. Circle: near center of wafer; square: near edge of wafer.

within each of the heating zones were resistive heating elements and temperature sensors. The zones were separated by a small air-gap of approximately 1 mm for thermal insulation.

Figure 3.10 shows the temperature and photoresist thickness for Wafer 14. Since no photoresist thickness control were implemented, the thickness at the 2 points did not converge.

In practice manufacturing process must be repeatable (May and Spanos, 2006). In Figures 3.6 and 3.7, photoresist were thicker and CD smaller at the centers of

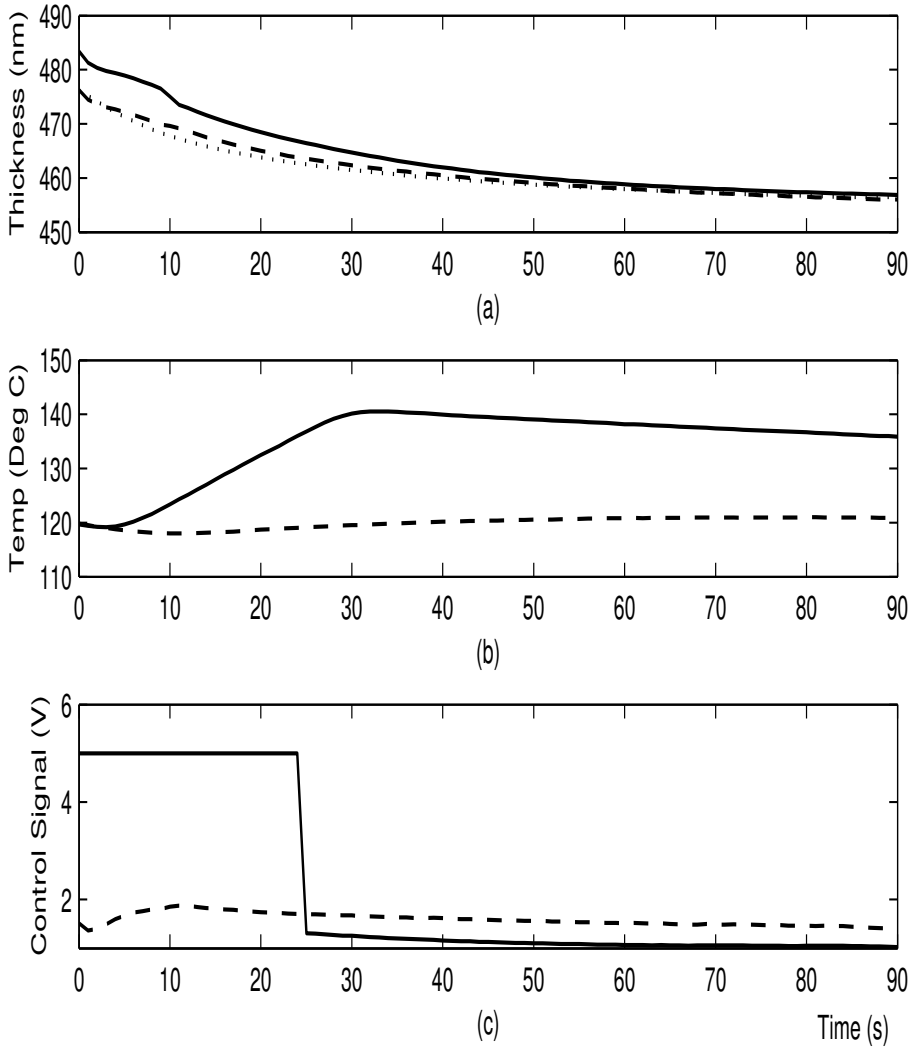


Fig. 3.8. Post-apply bake for Wafer 10 within-wafer CD control. (a) Photoresist thickness; (b) Bake plate temperature; (c) Control signal, u, in Voltage (V). Solid-line: near center of wafer; dashed-line: near edge of wafer; dotted-line: desired photoresist thickness.

Wafers 14 to 17 and 22 to 25. The photoresist thickness deviation and CD deviation between center and edge were about 5 nm and 20 nm respectively. Notice that in Figure 3.8, the edge was baked at about 120°C and the proportional-integral controller raised the temperature of the center to about 135°C. In practice, the 2 zones could be pre-programmed to start baking at these temperatures instead of waiting for the proportional-integral controller to change the temperature. Convergence to the desired thickness would be faster.

The thickness control method proposed in this Chapter can also be combined with the real-time temperature method proposed in Chapter 2. Real-time thickness control method can be applied during post-apply bake to reduce CD variation due to standing wave effect, while the real-time temperature control method can be applied to post-exposure bake. In this way, CD nonuniformity caused by standing wave effect and/or warpage can be reduced. Since warpage has no impact on resist thickness measurement (Tay and Wu, 2007), the thickness control method can also be applied for warped wafers.

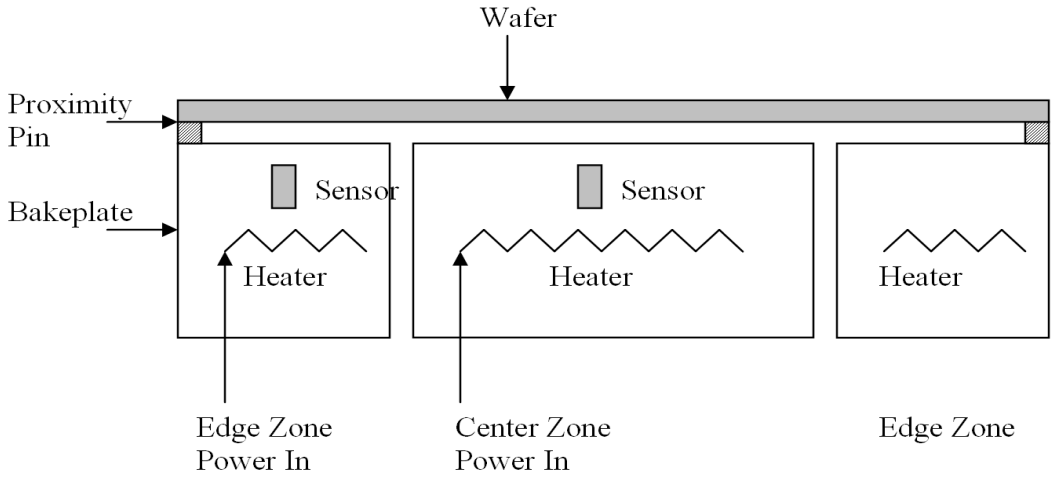


Fig. 3.9. Schematic diagram of a two-zone bake plate.

3.4 Conclusion

The experimental results on wafer-to-wafer and within-wafer CD control are presented. The CD non-uniformity can be reduced through real-time photoresist thickness control by manipulation of the post-apply bake temperature. The desired thickness was chosen such that it did not result in temperatures that were too high or too low. The experiments demonstrated a reduction of CD non-uniformity from about 20 nm to 2 nm for CD of 395 nm and 500 nm.

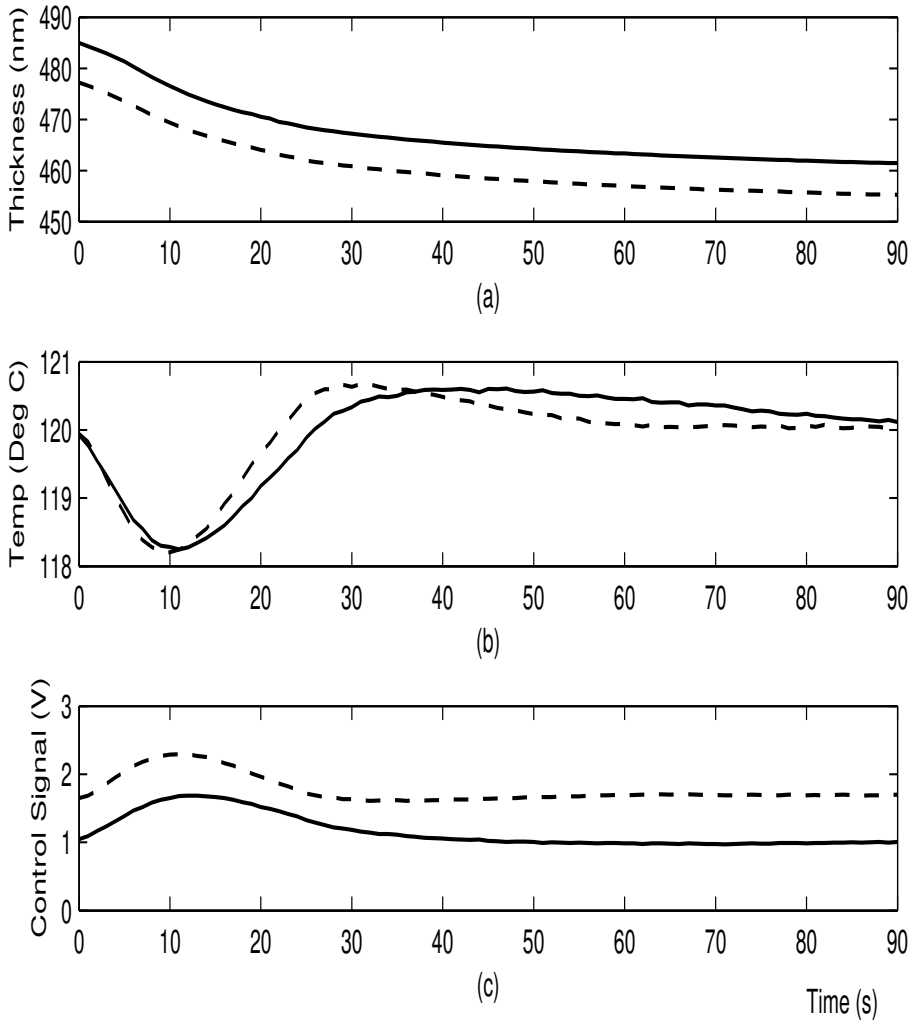


Fig. 3.10. Post-apply bake for Wafer 14 with no photoresist thickness control. (a) Photoresist thickness. (b) Bake plate temperature. (c) Control signal, u, in Voltage (V). Solid-line: near center of wafer; dashed-line: near edge of wafer.

Chapter 4

Optimal Feed-Forward Control for Multizone Baking

An algorithm for feed-forward control to improve the performance of a multizone baking system used for lithography in semiconductor manufacturing is derived in this Chapter. It uses linear programming optimization of the heat transfer in a multizone bake plate to produce a pre-determined heating sequence. The objective is to minimize the temperature disturbance induced by the placement of a wafer at ambient temperature on the hot multizone bake plate and the improvement is verified experimentally.

4.1 Introduction

As shown in Figure 1.1, the microlithography sequence includes numerous baking steps such as post-apply bake, post-exposure bake, and post-develop bake (Quirk

and Serda, 2001). In some cases, additional bake steps are used. Each of these bake steps serves different roles in transferring the latent image into the substrate. Of these, the most important or temperature sensitive is the post-exposure bake step. The post-exposure bake step is critical to current deep ultraviolet lithography. It is used to promote chemical modifications of the exposed portions of the photoresists. For such chemically amplified photoresists, the temperature of the wafer during this thermal step must be controlled to a high degree of precision for critical dimension control. The requirements call for temperature to be controlled to within $\pm$ 0.1°C at temperatures between 70°C and 150°C (Quirk and Serda, 2001).

A single-zone feed-forward controller was proposed by Ho *et al.* (2000) and Tay *et al.* (2004*b*) for a single-zone bake plate. The key idea was to accurately model the temperature drop of the bake plate that was caused by the placement of a wafer at room temperature on the hot bake plate and precisely calculate the extra power required to eliminate the temperature drop. The single-zone feed-forward controller eliminated the temperature disturbance caused by the placement of a cold wafer on a single-zone bake plate (Ho *et al.*, 2000; Tay *et al.*, 2004*b*).

The latest state-of-the-art bake plate uses multiple-zone heaters for various purposes, such as achieving resist thickness uniformity (using different post-apply bake temperature for different zones) (Lee *et al.*, 2002; Ho *et al.*, 2002) and improving critical dimension uniformity (using different post-exposure bake temperature for different zones) (Berger *et al.*, 2004*a*; Berger *et al.*, 2004*b*). However, when one applies the single-zone feed-forward algorithm from Ho *et al.* (2000) and Tay *et al.* (2004*b*) on the multizone bake plate, complete elimination of the temperature

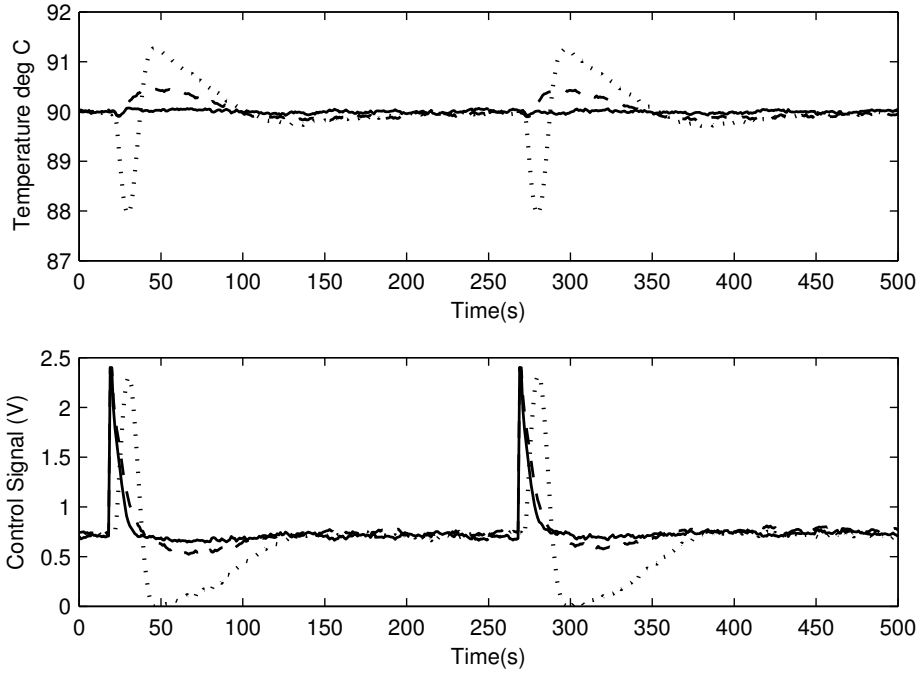
disturbance could not be achieved. The algorithm did not take into account heat transfer between the zones. Because of the fact that the algorithm was developed for a single-zone bake plate, heat was applied to all zones with the assumption of no neighboring zones. As a result, overheating occurred, because of heat that was transferred from neighboring zones. This accounts for the 0.5°C overheating at t = 50s and t = 300s in Figure 4.1 (see temperature curve, dashed-line).

In this Chapter, an algorithm for the multizone bake plate is developed. The new algorithm essentially eliminated the temperature disturbance as shown in Figure 4.1 (see temperature curve, solid-line).

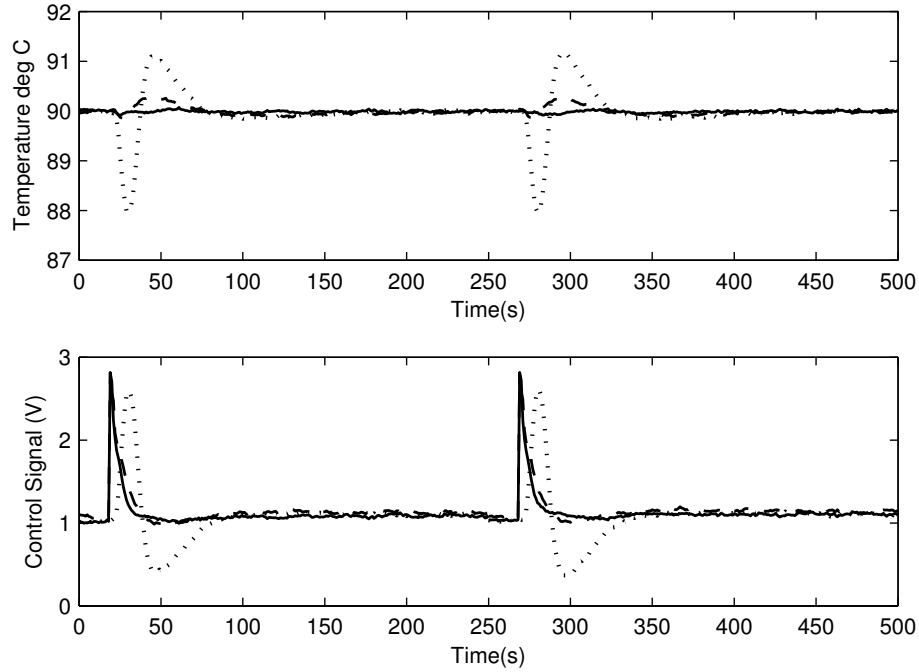
There is usually an error budget associated with the processing of the wafer. As the wafer goes through many processing steps, errors introduced in each step leads to error in the final critical dimension. For a specified error tolerance, large errors in other processing steps can be compensated by reducing the temperature errors introduced in the baking step.

4.2 Multizone Bake Plate Thermal Model

In this Section, a physical model will be derived for a multizone bake plate, based on heat transfer laws. As shown in Figure 4.2, the bake plate is formed by multiring zones, denoted as zone 1, 2, $\cdots$, m, from the inner zone to outer zone respectively. The wafer is considered to be formed by m zones also, with the same boundary as the bake plate. Because of the good heat conduction of metal and silicon, the temperature within each zone of wafer or bake plate is assumed to be



(a) Inner Zone



(b) Outer Zone

Fig. 4.1. Comparison of bake plate temperature disturbance caused by the placement of a cold wafer on the multizone bake plate. Solid-line: multizone feed-forward algorithm; dashed-line: single-zone feed-forward algorithm; dotted-line: proportional-integral feedback control only. 0∼250s one group of experiments; 250∼500s, repetitive experiments

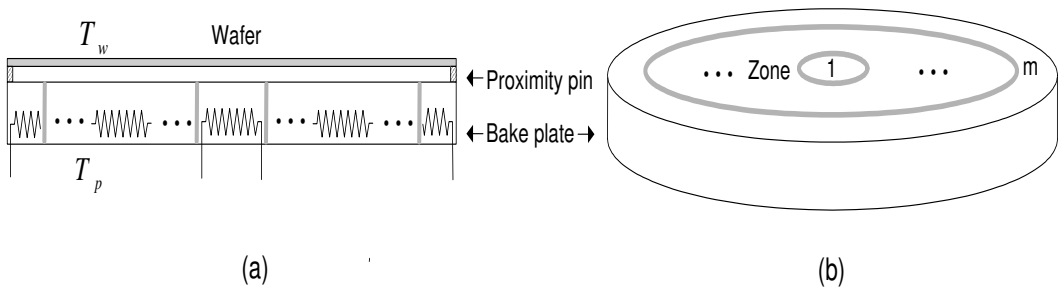


Fig. 4.2. Schematic Diagram of the multizone bake plate

sufficiently uniform. Thus a distributed lumped model can satisfactorily describe the plant characteristics. Given the energy balance and heat transfer law, the bake plate can be modeled as

$$\begin{aligned} C_{wi}\dot{T}_{wi}(t) &= \frac{T_{pi}(t)-T_{wi}(t)}{r_{ai}} + \frac{T_{w(i-1)}(t)-T_{wi}(t)}{r_{w(i-1)i}} \\ &\quad -\frac{T_{wi}(t)}{r_{wi}} + \frac{T_{w(i+1)}(t)-T_{wi}(t)}{r_{wi(i+1)}} \end{aligned} \tag{4.1}$$

$$\begin{aligned} C_{pi}\dot{T}_{pi}(t) &= p_i(t) + \frac{T_{wi}(t)-T_{pi}(t)}{r_{ai}} + \frac{T_{p(i-1)}(t)-T_{pi}(t)}{r_{p(i-1)i}} \\ &\quad -\frac{T_{pi}(t)}{r_{pi}} + \frac{T_{p(i+1)}(t)-T_{pi}(t)}{r_{pi(i+1)}} \end{aligned} \tag{4.2}$$

where

i	parameter for zone i ($i = 1, 2, \cdots, m$)
C_w	heat capacity of wafer (J/K)
C_p	heat capacity of bake plate (J/K)
$T_w(t)$	wafer temperature above ambient (K)
$T_p(t)$	bake plate temperature above ambient (K)

r_a thermal resistance between wafer and bake plate (K/W)

r_w thermal resistance between wafer and surrounding air

r_p thermal resistance between bake plate and surrounding air

$r_{w(i-1)i}$ thermal resistance between wafer zone $i-1$ and zone i;

$r_{w(i-1)i} = \infty$ for $i = 1$ (K/W)

$r_{wi(i+1)}$ thermal resistance between wafer zone i and zone $i+1$;

$r_{wi(i+1)} = \infty$ for $i = m$ (K/W)

$r_{p(i-1)i}$ thermal resistance between bake plate zone $i-1$ and zone i;

$r_{p(i-1)i} = \infty$ for $i = 1$ (K/W)

$r_{pi(i+1)}$ thermal resistance between bake plate zone i and zone $i+1$;

$r_{pi(i+1)} = \infty$ for $i = m$ (K/W)

$p(t)$ heater power (W)

At steady state, $\dot{T}_{wi}(\infty) = \dot{T}_{pi}(\infty) = 0$ and Equations (4.1) and(4.2) become

$$\begin{aligned}\left(\frac{1}{r_{ai}}\right) T_p i(\infty) &= \left(\frac{1}{R_{wi}}\right) T_{wi}(\infty) - \left(\frac{1}{r_{w(i-1)i}}\right) T_{w(i-1)}(\infty) \\ &\quad - \left(\frac{1}{r_{wi(i+1)}}\right) T_{w(i+1)}(\infty) \qquad (4.3)\\ p_i(\infty) &= -\left(\frac{1}{r_{ai}}\right) T_{wi}(\infty) - \left(\frac{1}{r_{p(i-1)i}}\right) T_{p(i-1)}(\infty) \\ &\quad + \left(\frac{1}{R_{pi}}\right) T_{pi}(\infty) - \left(\frac{1}{r_{pi(i+1)}}\right) T_{p(i+1)}(\infty) \qquad (4.4)\end{aligned}$$

where

$$\begin{aligned}\frac{1}{R_{wi}} &= \frac{1}{r_{ai}} + \frac{1}{r_{wi}} + \frac{1}{r_{w(i-1)i}} + \frac{1}{r_{wi(i+1)}} \\ \frac{1}{R_{pi}} &= \frac{1}{r_{ai}} + \frac{1}{r_{pi}} + \frac{1}{r_{p(i-1)i}} + \frac{1}{r_{pi(i+1)}}\end{aligned}$$

Defining new variables ($\theta_{wi}(t) = T_{wi}(t) - T_{wi}(\infty)$, $\theta_{pi}(t) = T_{pi}(t) - T_{pi}(\infty)$, and $u_i(t) = p_i(t) - p_i(\infty)$) and substituting Equations (4.3) and (4.4) into Equations (4.1) and (4.2) gives

$$\begin{aligned} C_{wi}\dot{\theta}_{wi}(t) &= \left(\frac{1}{r_{w(i-1)i}}\right)\theta_{w(i-1)}(t) - \left(\frac{1}{R_{wi}}\right)\theta_{wi}(t) \\ &\quad + \left(\frac{1}{r_{wi(i+1)}}\right)\theta_{w(i+1)}(t) + \left(\frac{1}{r_{ai}}\right)\theta_{pi}(t) \qquad (4.5) \\ C_{pi}\dot{\theta}_{pi}(t) &= u_i(t) + \left(\frac{1}{r_{ai}}\right)\theta_{wi}(t) + \left(\frac{1}{r_{p(i-1)i}}\right)\theta_{p(i-1)}(t) \\ &\quad - \left(\frac{1}{R_{pi}}\right)\theta_{pi}(t) + \left(\frac{1}{r_{pi(i+1)}}\right)\theta_{p(i+1)}(t) \qquad (4.6) \end{aligned}$$

Equations (4.5) and (4.6)can be written in a state-space model

$$\dot{x} = Fx + Gu \qquad (4.7)$$

$$y = Hx \qquad (4.8)$$

where

$$\begin{aligned} x &= [\theta_{w1}\ \theta_{w2}\ \cdots\ \theta_{wm}\ \theta_{p1}\ \theta_{p2}\ \cdots\ \theta_{pm}]^T \\ u &= [u_1\ u_2\ \cdots\ u_m]^T \\ y &= [\theta_{p1}\ \theta_{p2}\ \cdots\ \theta_{pm}]^T \end{aligned}$$

$$
\begin{aligned}
G &= \begin{bmatrix} 0 & & 0 \\ & \ddots & \\ 0 & & 0 \\ \frac{1}{C_{p1}} & & \\ & \ddots & \\ 0 & & \frac{1}{C_{pm}} \end{bmatrix} \\
H &= \begin{bmatrix} 0 & & 0 & 1 & & 0 \\ & \ddots & & & \ddots & \\ 0 & & 0 & 0 & & 1 \end{bmatrix} \\
F &= \begin{bmatrix} P & Q \\ R & S \end{bmatrix}
\end{aligned}
$$

and $P,\ Q,\ R,\ S$ are $m \times m$ matrix given by

$$
P = \begin{bmatrix}
-\frac{1}{R_{w1}C_{w1}} & \frac{1}{r_{w12}C_{w1}} & & & 0 \\
\frac{1}{r_{w12}C_{w2}} & -\frac{1}{R_{w2}C_{w2}} & \frac{1}{r_{w23}C_{w2}} & & \\
 & \frac{1}{r_{w23}C_{w3}} & \ddots & \ddots & \\
 & & \ddots & \ddots & \frac{1}{r_{w(m-1)m}C_{w(m-1)}} \\
0 & & & \frac{1}{r_{w(m-1)m}C_{wm}} & -\frac{1}{R_{wm}C_{wm}}
\end{bmatrix}
$$

$$Q = \begin{bmatrix} \frac{1}{r_{a1}C_{w1}} & & 0 \\ & \ddots & \\ 0 & & \frac{1}{r_{am}C_{wm}} \end{bmatrix}$$

$$R = \begin{bmatrix} \frac{1}{r_{a1}C_{p1}} & & 0 \\ & \ddots & \\ 0 & & \frac{1}{r_{am}C_{pm}} \end{bmatrix}$$

$$S = \begin{bmatrix} -\frac{1}{R_{p1}C_{p1}} & \frac{1}{r_{p12}C_{p1}} & & & 0 \\ \frac{1}{r_{p12}C_{p2}} & -\frac{1}{R_{p2}C_{p2}} & \frac{1}{r_{p23}C_{p2}} & & \\ & \frac{1}{r_{p23}C_{p3}} & \ddots & \ddots & \\ & & \ddots & \ddots & \frac{1}{r_{p(m-1)m}C_{p(m-1)}} \\ 0 & & & \frac{1}{r_{p(m-1)m}C_{pm}} & -\frac{1}{R_{pm}C_{pm}} \end{bmatrix}$$

4.3 Multizone Feed-forward Control

The objective is to eliminate the temperature disturbance caused by the placement of a cold wafer on the multizone bake plate. The feed-forward control algorithm derived in this section takes heat transfer between neighboring zones into considerations.

Discretizing with sampling interval h, the state-space model of the multizone

bake plate in Equations (4.7) and (4.8) is given by

$$x(k+1) = \Phi x(k) + \Gamma u(k) \tag{4.9}$$

$$y(k) = Hx(k) \tag{4.10}$$

where

$$\begin{aligned}
\Phi &= e^{Fh} \\
\Gamma &= \int_0^h e^{Fh} d\eta G \\
x(k) &= [\theta_{w1}(k)\ \theta_{w2}(k)\ \cdots\ \theta_{wm}(k)\ \theta_{p1}(k)\ \theta_{p2}(k)\ \cdots\ \theta_{pm}(k)]^T \\
u(k) &= [u_1(k)\ u_2(k)\ \cdots\ u_m(k)]^T \\
y(k) &= [\theta_{p1}(k)\ \theta_{p2}(k)\ \cdots\ \theta_{pm}(k)]^T
\end{aligned}$$

Assuming that the initial temperature of the wafer and bake plate, $x(0)$, and the control signals $u(0), u(1), \cdots, u(N-1)$ are given, it is possible to solve Equations (4.9) and (4.10) using simple iterations.

$$\begin{aligned}
x(1) &= \Phi x(0) + \Gamma u(0) \\
y(1) &= H(\Phi x(0) + \Gamma u(0)) \\
x(2) &= \Phi^2 x(0) + \Phi\Gamma u(0) + \Gamma u(1) \\
y(2) &= H(\Phi^2 x(0) + \Phi\Gamma u(0) + \Gamma u(1)) \\
&\vdots \\
x(N) &= \Phi^N x(0) + \Phi^{N-1}\Gamma u(0) + \Phi^{N-2}\Gamma u(1) + \cdots + \Gamma u(N-1) \\
y(N) &= H(\Phi^N x(0) + \Phi^{N-1}\Gamma u(0) + \Phi^{N-2}\Gamma u(1) + \cdots + \Gamma u(N-1))
\end{aligned}$$

The solution consists of two parts:

$$Y = D + \Psi U$$

D is dependent on the initial wafer and bake plate temperatures, and ΨU is the control signal.

$$Y = \begin{bmatrix} y(1) \\ y(2) \\ \vdots \\ y(N) \end{bmatrix}$$

$$U = \begin{bmatrix} u(0) \\ u(1) \\ \vdots \\ u(N-1) \end{bmatrix}$$

$$\Psi = \begin{bmatrix} \psi(1) \\ \psi(2) \\ \vdots \\ \psi(N) \end{bmatrix} = \begin{bmatrix} H\Gamma & 0 & \cdots & \cdots & 0 \\ H\Phi\Gamma & H\Gamma & 0 & \cdots & 0 \\ \vdots & \vdots & & & \vdots \\ H\Phi^{N-1}\Gamma & H\Phi^{N-2}\Gamma & \cdots & \cdots & H\Gamma \end{bmatrix}$$

$$D = \begin{bmatrix} H\Phi \\ H\Phi^2 \\ \vdots \\ H\Phi^N \end{bmatrix} x(0)$$

The effect of the disturbance D caused by the ambient wafer temperature in

$x(0)$ can be eliminated if

$$Y = D + \Psi U = 0$$

When there is no constraint on the control signal, the disturbance can be rejected totally if the control signal is computed as

$$U = -\Psi^{-1} D$$

However, in practice, the power is subjected to lower and upper limits, i.e., $u \in [u_{min}, u_{max}]$ and the objective function can be optimized,

$$\min_{u \in [u_{min}, u_{max}]} \max |D + \Psi U| \tag{4.11}$$

The optimization problem of equation (11) is equivalent to the following linear programming problem:

$$\text{Min} \begin{bmatrix} 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} U \\ \\ e \end{bmatrix} \qquad \text{(objective function)}$$

subject to

$$\begin{bmatrix} \Psi & -1_I \\ \\ -\Psi & -1_I \end{bmatrix} \begin{bmatrix} U \\ \\ e \end{bmatrix} \leq \begin{bmatrix} -D \\ \\ D \end{bmatrix} \qquad \text{(dynamic model)}$$

$U \leq U_{max}$ (upper control signal limit)

$U \geq U_{min}$ (lower control signal limit)

$\psi(k)U + D(k) = 0$ ($k \in [n_f, \cdots, N]$; disturbance eliminated from n_f onwards)

where 1_I is a column vector with all entries equal to 1, and

$U_{max} = [u_{1\_max}\ u_{2\_max}\ \cdots\ u_{m\_max}\ u_{1\_max}\ u_{2\_max}\ \cdots\ u_{m\_max}\ \cdots]^T$

$$U_{min} = [u_{1\_min}\ u_{2\_min}\ \cdots\ u_{m\_min}\ u_{1\_min}\ \ u_{2\_min}\ \cdots\ u_{m\_min}\ \cdots]^T$$

where U_{max} and U_{min} are $m \times N$ rows vectors, u_{i_max} and u_{i_min} respectively denote the upper and lower bounds of the i heater power respectively. For vectors v and w, $v \leq w$ means every element of v is less than or equal to the corresponding element of w. The parameter n_f is chosen such that n_f is valid while n_{f-1} is not.

4.4 Experimental Results

In this Section, the feed-forward control strategy is demonstrated on a two-zone ($m = 2$) bake plate for a 200mm wafer. A photograph of the bake plate is shown in Figure 4.3. Two resistance temperature devices were used to measure the temperature. Room temperature was 24.5°C, and the experiments were conducted at a set-point of 90°C with a sampling interval of $h = 1$ s. For a two-zone bake plate, the model is reduced to

$$C_{w1}\dot{T}_{w1}(t) = \frac{T_{p1}(t) - T_{w1}(t)}{r_{a1}} - \frac{T_{w1}(t)}{r_{w1}} + \frac{T_{w(2)}(t) - T_{w1}(t)}{r_{w12}} \quad (4.12)$$

$$C_{w2}\dot{T}_{w2}(t) = \frac{T_{p2}(t) - T_{w2}(t)}{r_{a2}} + \frac{T_{w1}(t) - T_{w2}(t)}{r_{w12}} - \frac{T_{w2}(t)}{r_{w2}} \quad (4.13)$$

$$C_{p1}\dot{T}_{p1}(t) = p_1(t) + \frac{T_{w1}(t) - T_{p1}(t)}{r_{a1}} - \frac{T_{p1}(t)}{r_{p1}} + \frac{T_{p2}(t) - T_{p1}(t)}{r_{p12}} \quad (4.14)$$

$$C_{p2}\dot{T}_{p2}(t) = p_2(t) + \frac{T_{w2}(t) - T_{p2}(t)}{r_{a2}} + \frac{T_{p1}(t) - T_{p2}(t)}{r_{p12}} - \frac{T_{p2}(t)}{r_{p2}} \quad (4.15)$$

where subscript "1" denotes inner zone and and subscript "2" denotes outer zone. The parameters of the bake plate and wafer are given below.

For the wafer:

Inner zone radius: $r_1 = 60$ mm

Outer zone radius: $r_2 = 100$ mm

Wafer thickness: $d_w = 750$ μm

Natural convection coefficient: $h_w = 10.0$ W/(m^2 K)

Surface area: $A_w = \pi r_2^2 = 0.0314$ m^2

Surface area of the inner zone: $A_{w1} = \pi r_1^2 = 0.0113$ m^2

Surface area of the outer zone: $A_{w2} = \pi(r_2^2 - r_1^2) + 2\pi r_2 d_w = 0.0206$ m^2

Heat capacity of the inner zone: $C_{w1} = 16.92$ J/K

Heat capacity of the outer zone: $C_{w2} = 30.08$ J/K

For the bake plate:

Air gap thickness: $l_a = 70$ μm

Thermal conductivity of air: $k_a = 0.03$ W/(m K)

Natural convection coefficient: $h_p = 7.4$ W/(m^2 K)

Surface area of the inner zone: $A_{p1} = 0.0113$ m^2

Surface area of the outer zone: $A_{p2} = 0.0591$ m^2

Heat capacity of the inner zone: $C_{p1} = 359.4$ J/K

Heat capacity of the outer zone: $C_{p2} = 638.9$ J/K

Thermal resistances are given as follows:

$r_{a1} = \frac{l_a}{k_a A_{w1}} = 0.206$ K/W

$r_{a2} = \frac{l_a}{k_a A_{w2}} = 0.116$ K/W

$r_{w1} = \frac{1}{h_w A_{w1}} = 8.842$ K/W

$r_{w2} = \frac{1}{h_w A_{w2}} = 4.860$ K/W

$r_{w12} = 0.013$ K/W

$r_{p1} = \frac{1}{h_p A_{p1}} = 11.949$ K/W

Fig. 4.3. Photograph of the multizone bake plate

$r_{p2} = \frac{1}{h_p A_{p2}} = 2.286$ K/W

$r_{p12} = 0.17$ K/W

The thermal resistances r_{w12} and r_{p12} between inner zone and outer zone was calculated using Equations (4.3) and (4.4), with $T_{p1}(\infty) = 66.2$°C, $T_{w1}(\infty) = 64.25$°C, $T_{p2}(\infty) = 65.5$°C, $T_{w2}(\infty) = 64.22$°C, $p_1(\infty) = 19.11$W, $p_2(\infty) = 35.56$W.

Based on the aforementioned parameters, the bake plate model is given as

$$F = \begin{bmatrix} -4.8389 & 4.5458 & 0.2864 & 0 \\ 2.5570 & -2.8503 & 0 & 0.2864 \\ 0.01349 & 0 & -0.03008 & 0.01636 \\ 0 & 0.01349 & 0.009205 & -0.02338 \end{bmatrix}$$

$$G = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0.002782 & 0 \\ 0 & 0.001565 \end{bmatrix}$$

$$H = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\Phi = \begin{bmatrix} 0.269523 & 0.477930 & 0.112746 & 0.133872 \\ 0.268836 & 0.478601 & 0.075318 & 0.171281 \\ 0.005309 & 0.006305 & 0.971344 & 0.016767 \\ 0.003546 & 0.008065 & 0.009431 & 0.978239 \end{bmatrix}$$

$$\Gamma = \begin{bmatrix} 0.000188 & 0.000097 \\ 0.000097 & 0.000148 \\ 0.002742 & 0.000013 \\ 0.000013 & 0.001548 \end{bmatrix}$$

$$x(0) = \begin{bmatrix} -63.99 & -63.98 & 0 & 0 \end{bmatrix}^T$$

The optimal feed-forward control signal, U, was computed for the objective

function (11), using linear programming and the constraints $u_{1_min} = -12.8$W, $u_{2_min} = -41.7$W, $u_{1_max} = 240$W, $u_{2_max} = 420$W. Note that a time delay of 4 s was present; this corresponded to the time delay for the heater power to reach the surface of the plate. Therefore, the feed-forward control signal U was applied 4 s before the placement of the wafer. Here, the steady-state powers $p_1(\infty) = 12.8$ W and $p_2(\infty) = 41.7$ W. Besides the feed-forward control signals, two proportional-integral feedback controllers of the form

$$G_{c1} = K_{p1}\left(1 + \frac{1}{sT_{i1}}\right) = 70\left(1 + \frac{1}{50s}\right)$$

$$G_{c2} = K_{p2}\left(1 + \frac{1}{sT_{i2}}\right) = 126\left(1 + \frac{1}{50s}\right)$$

were used for the inner zone heater and outer zone heater, respectively. In discrete form, they are given as

$$\begin{aligned} G_{c1}(q^{-1}) &= \frac{70 - 68.6q^{-1}}{1 - q^{-1}} \\ G_{c2}(q^{-1}) &= \frac{126 - 123.48q^{-1}}{1 - q^{-1}} \end{aligned}$$

The new algorithm eliminated the temperature disturbances at $t = 50$s and $t = 300$s as shown in Figure 4.1 (see temperature curve, solid-line). The thermal coupling between the inner zone and outer zone was considered in the new algorithm. r_{w12} represents the thermal resistance between inner wafer zone and outer wafer zone, while r_{p12} represents the thermal resistance of inner bake plate zone and outer bake plate zone. For single zone algorithm, the heating transfer between neighbouring zones are ignored, thus $r_{w12} = \infty$ and $r_{p12} = \infty$. Current control schemes for the baking processes are usually proportional-integral feedback

Table 4.1. Comparison of the settling time, temperature deviation and integrated square error for multizone and single-zone feed-forward control algorithm

parameter	Multizone Algorithm		Single-zone Algorithm		PI Control Only	
	Inner	Outer	Inner	Outer	Inner	Outer
settling time (s)	0	0	200	108	167	120
temp. deviation (°C)	+0.06	+0.06	+0.45	+0.29	+1.26	+1.15
	−0.08	−0.09	−0.19	−0.14	−2.07	−2.04
ISE	0.2079	0.1747	8.1604	1.9690	71.9116	50.1348

controller provided by the bake plate vendors. The feedback information is the error between bake plate temperature and the setpoint, which is around 0 initially. When wafer is dropped onto the bake plate, the PI controller increases the input power gradually as the error increases. The controller response is slower compared with Feed-forward controller which provides a big power increase immediately at time of wafer drop. Thus existing PI control systems can't reject the temperature disturbance totally.

Table 1 shows the comparison of the multizone feed-forward algorithm, single-zone feed-forward algorithm, and proportional-integral feedback control without any feed-forward. The readings in Table 1 are the average of the 2 disturbances in Figure 4.1. The multizone feed-forward algorithm has reduced temperature disturbance of the single-zone algorithm from peak-to-peak value of 0.6°C (−0.19 to 0.45) to 0.15°C (−0.09 to 0.06). There is an order-of-magnitude improvement in the integrated square error (ISE), from 1.9 to 0.2. The settling time, which is defined as the time required for the temperature disturbance to settle to less than ± 0.1°C is reduced to 0 s. The typical PEB processing time is around 60s∼120s. For the single zone feed-forward algorithm, and PI feedback control, the settling

time will be longer than the processing time for most photoresist. The temperature processing trajectory will be different wafer-to-wafer, otherwise the cycle time will be increased waiting bake plate temperature to settle down. Wafer-to-wafer temperature trajectory variation will result in wafer-to-wafer CD nonuniformity during PEB where CD is very sensitive to temperature.

4.5 Conclusion

Requirements for critical thermal processing steps in microlithography call for temperature to be controlled to within $\pm$ 0.1°C. An algorithm for the feed-forward control of the multizone bake plate is given in this Chapter. It takes into account the heat transfer between neighboring zones and almost eliminated the temperature disturbance caused by the placement of a cold wafer on the bake plate.

Chapter 5

Conclusion

5.1 Summary of Results

One trend in lithography is to implement advanced control and signal processing techniques to meet requirements for both development and volume manufacturing. CD control is particularly a major challenge. This thesis examines the application of advanced control algorithms in various baking processes to meet some stringent requirements, mainly on the CD control. Three areas of applications have been discussed: real-time CD and temperature control for warped wafers during PEB, real-time CD and thickness control, and optimal feed-forward control for thermal processing of wafers. The results are summarized as follows.

In Chapter 2, a real-time temperature control method was implemented to improve CD uniformity for warped wafers. Wafer warpage results in CD nonuniformity due to the air-gap variation between wafer and bake plate. A double-zone bake plate was used to heat the wafer center zone and edge zone respectively

during PEB. Shipley UVIII was used in the experiment. For flat wafers with conventional bake, the within-wafer CD nonuniformity was around 23nm. To obtain uniform CD for flat wafers, the bake plate temperature profiles were optimized. CD nonuniformity between the center and edge was improved to around 2nm. For wafers with 140μm center-to-edge warpage, the within-wafer CD nonuniformity was doubled to 46nm with conventional bake. To obtain uniform CD for warped wafers, the real-time temperature control strategy is implemented on the double-zone bake plate. For warped wafers, bake plate temperature setpoint was adjusted online immediately after the maximum bake plate temperature drops. Experimental results showed that the within-wafer CD nonuniformity was reduced to around 2nm for warped wafers. In addition, the nonuniformity between warped wafers and flat wafers (wafer-to-wafer) was reduced to around 2nm. As a comparison, the wafer-to-wafer nonuniformity with conventional bake was 37nm for the center and 13.5nm for the edge respectively.

In Chapter 3, a real-time resist thickness control method was presented to improve resist thickness and CD uniformity in lithography. For conventional bake with bake plate temperature regulated to a fix setpoint, both the thickness and final CD were nonuniform in terms of wafer-to-wafer and within-wafer. With the thickness control method, resist thickness was monitored with a spectrometer. The thickness was controlled to follow a pre-determined trajectory by manipulating the heating power in real-time. Experimental results showed that both wafer-to-wafer and within-wafer thickness nonuniformity was reduced to less than 1nm and CD nonuniformity was improved to around 2nm.

An optimal feed-forward control method was proposed for thermal processing of wafers on the multizone bake plate in Chapter 4. When wafer at room temperature is dropped onto the bake plate, there is a disturbance to the bake plate temperature. The objective of the optimal feed-forward controller is to minimize the worse case deviation. The optimal feed-forward control signals can be derived by solving a linear programming problem. The method was implemented on a double-zone bake plate, and experimental results showed that the bake plate temperature disturbance of both zones were reduced to less than 0.1°C. For conventional PI feedback control, however, the temperature disturbance amounts to 2°C. The superiority of the method is obvious in terms of temperature deviation, settling time and integrated square error when compared to two other methods.

5.2 Future Works

In the real-time temperature control strategy for PEB processing of warped wafers, it is demonstrated that it is possible to detect wafer warpage from the maximum temperature drop of the bake plate. Accuracy is expected to improve if more sophisticated estimation technique is used. One elaborate method is to fit the complete temperature trajectory of the bake plate with the model in the least square sense. A thermal model can be derived, with the air-gap between the wafer and bake plate unknown, which depends on the warpage. Once the wafer is put on the bake plate the temperature begins to drop. The warpage can be estimated by fitting the model output to measurement. On the next sampling, the warpage

can be updated recursively with more measurements available.

Further improvement can be expected if the wafer temperature variation before the maximum drop is taken into considerations. This effect is ignored in the thesis since this period is short (around 10s) compared to normal baking cycle time (1∼several minutes). In addition, the wafer temperature during this initial period is low and activation on the chemical reaction is small compared to the high temperature region. While for future lithography when requirements on CD variation become more and more stringent, considering the initial stage will further improve the performance. A possible solution is to implement combined feed-forward and feedback control strategy. Wafer warpage can detected during the post-apply bake, and forwarded to the PEB process where CD is more sensitive to warpage. The bake plate setpoints can be initially adjusted before the wafer arrives. When the wafer arrives for PEB processing, fine adjustment can be accomplished using the real time control method proposed in this thesis since warpage may change somewhat during the intermediate process. The integration of the feed-forward information will further reduce wafer temperature variation.

Optical metrology has been implemented in post-apply bake to improve resist thickness and CD uniformity. With more and more optical metrologies available, real-time monitoring and control of resist properties in PEB becomes possible. Deprotection of resist is strongly related to the pattern CD. The optical absorption and reflection index of resist changes once deprotected. Thus optical metrology such as scatterometer can be used to monitor the profile of deprotected area. For chemically amplified resist, the deprotection is greatly affected by the bake plate

temperature. With optical metrology integrated in-situ, real-time control of the resist deprotection can be realized by manipulating the PEB temperature. CD uniformity improvement can be expected.

The focus of this thesis is on the bake processes in lithography. CD uniformity can also be improved by real time control of the development processes. This is because the development process is also a strong function of temperature. Tay *et al.* (2007*b*) reported a real time control of the development rate for bulk resist. In practice there are usually patterns in the resist. A more advanced data analysis is required to monitor the development rate. The effects of the pattern on the reflectance signal must be considered to extract the development rate.

In the thermal processing of wafers, the optimal feed-forward control signals can be obtained by solving a liner programming problem to reject load disturbance. The feed-forward control problem can also be formulated as a minimum time control problem. The solution of the minimum time control problem boils down to finding the roots of equations which is much faster than solving a linear programming problem. Furthermore, a linear programming solver need not be made available. This makes it more suitable for online implementation. Tay *et al.* (2001) implemented the minimum time control on a single zone bake plate. The results can be extended to the multizone bake plate. However, the thermal coupling between neighbouring zones should be considered when solving the optimal control signals.

During thermal processing, the temperature deviation of warped wafers is expected to be bigger than flat wafers. In this case, controlling bake plate temperature to its former setpoints can no longer assure CD uniformity. Instead, optimal feed-forward control can be combined with the real-time temperature control method for warped wafers proposed in Chapter 2. The objective is to reduce disturbance during setpoint change.

Author's Publications

Award

The following paper received "Honorable Mention" in the Student Paper Competition:

Chen, Ming, Weng Khuen Ho, Arthur Tay, Jun Fu, Real Time Control of Resist Thickness and Critical Dimension Uniformity, AEC/APC Symposium XIX, India Wells, CA, USA, Sep 17-19, 2007

Journal Papers

Ho, Weng Khuen, Arthur Tay, Ming Chen, and Choon Meng Kiew (2007), Optimal Feed-Forward Control for Multizone Baking in Microlithography, *Industrial & Engineering Chemistry Research* 46(11), 3623-3628

Ho, Weng Khuen, Arthur Tay, Ming Chen, Jun Fu, Haijing Lu, Xuechuan Shan (2007), Critical Dimension Uniformity via Real-Time Photoresist Thicknesss Control, *IEEE Transactions on Semiconductor Manufacturing* 20(4), 376-380

Ho, Weng Khuen, Arthur Tay, Jun Fu, Ming Chen, Yong Feng, Critical Dimension

and Real-Time Temperature Control for Warped Wafers, accepted for publication in *Journal of Process Control*

Conference Papers

Ho, Weng Khuen, Arthur Tay, Jun Fu, Ming Chen, Critical Dimension Uniformity in Lithography: In-situ Thermal Compensation, IFAC Workshop on Advanced Process Control for Semiconductor Manufacturing, Singapore, December 4 - 5, 2006

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