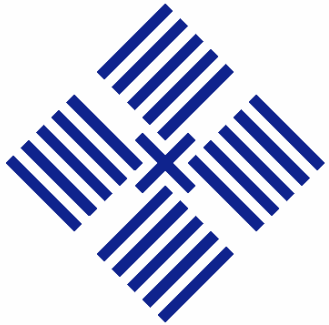

3DAlign™: Recent developments in double sided alignment and back-side alignment

ASML 200mm/Special Applications - SPIE Technical Symposium
February 28, 2007

Overview

- Concept & hardware
- Back-to-back Alignment Performance & Cost reduction
- Front-to-back Alignment Performance & Metrology
- Front-to-back Alignment on Glass Carriers

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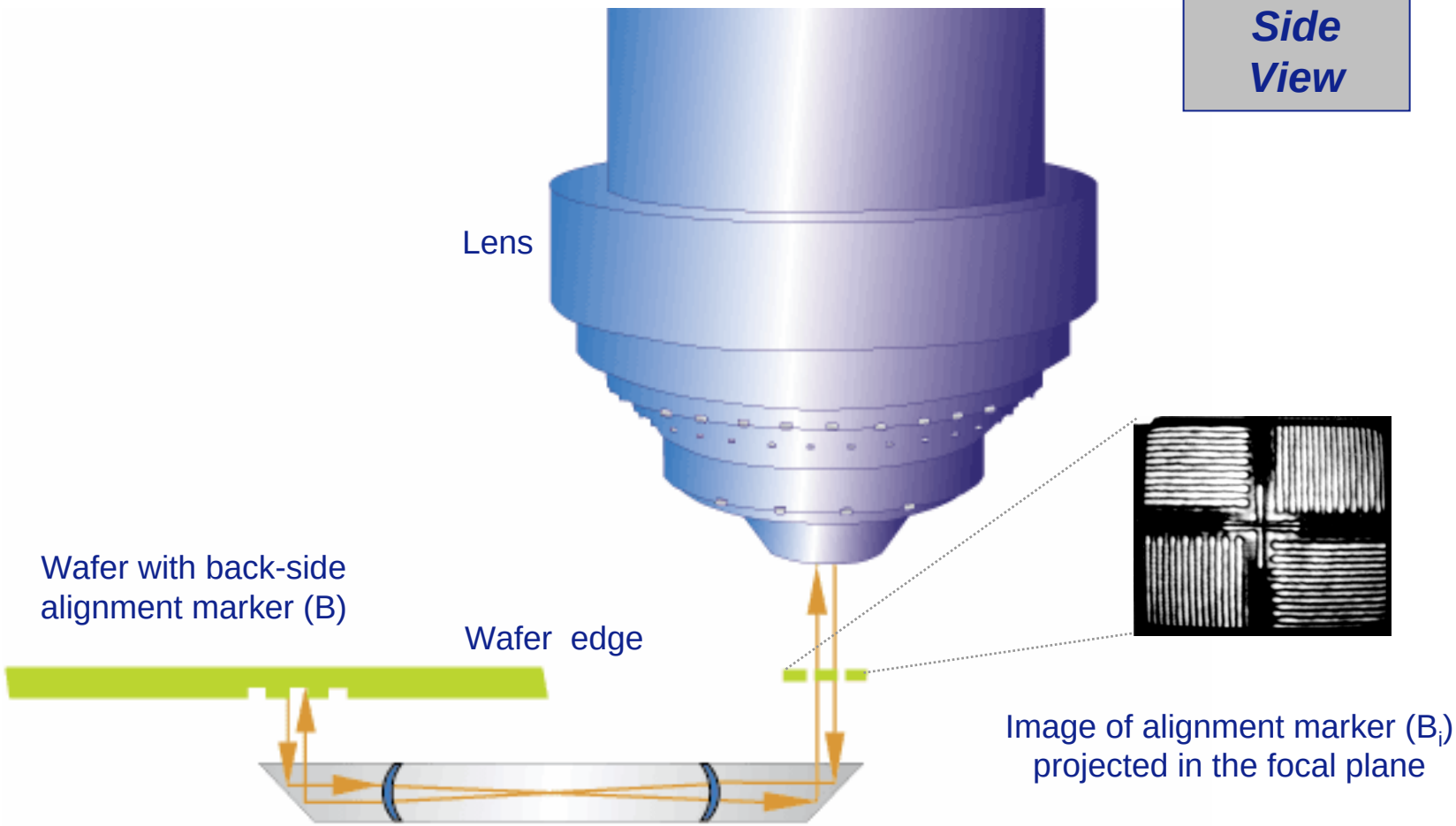
- Front-to-back Alignment on Glass Carriers

Concept

How does 3DAlign™ work?



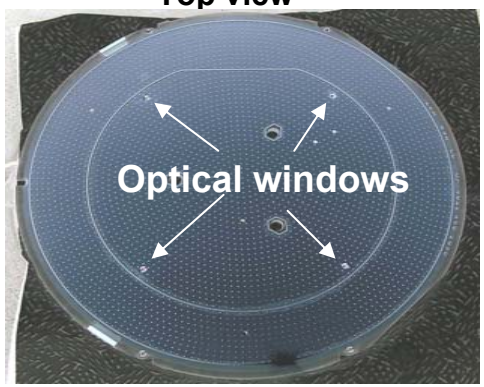
One of the built-in optical modules embedded in the wafer table, extending outside the wafer edge

Concept

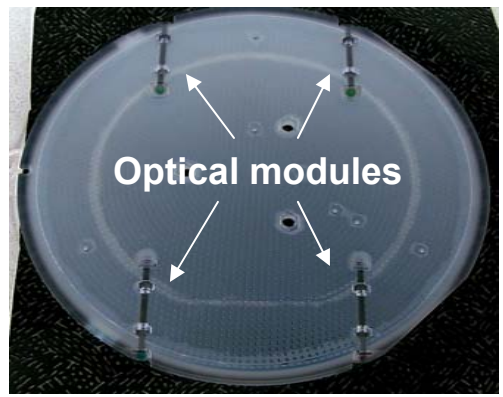
How does 3DAlign™ work?

Overview

Top view



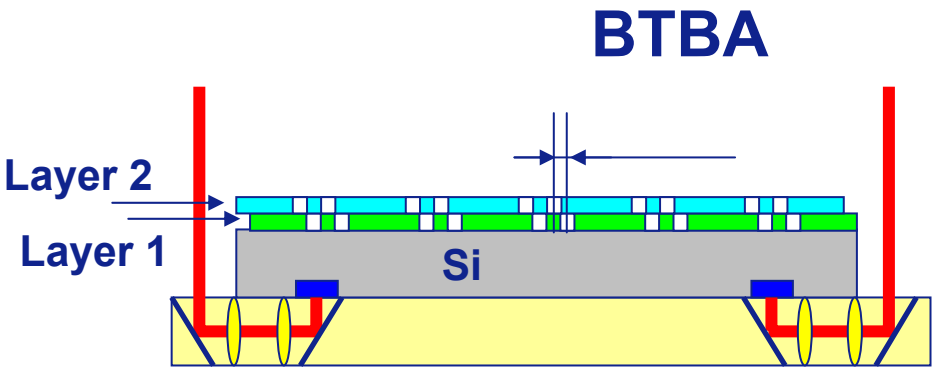
dedicated wafer exposure table with built-in optics



Bottom view

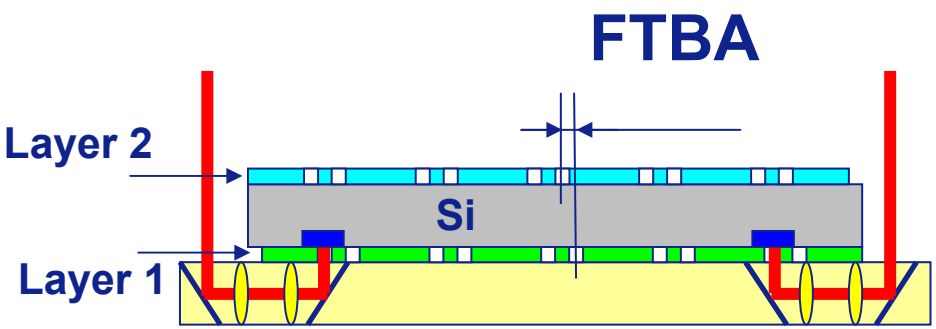
- Use existing TTL alignment capability of ASML tool + 3DAlign™ upgrade
- Use existing reticle set, choose for front-side or back-side alignment per layer

3DAlign™ Overlay definitions



Back-to-back alignment

- Allows for decoupling the process from alignment
- IC applications, etc



Front-to-back alignment

- Double sided alignment
- MEMS, compound, 3D-IC, etc

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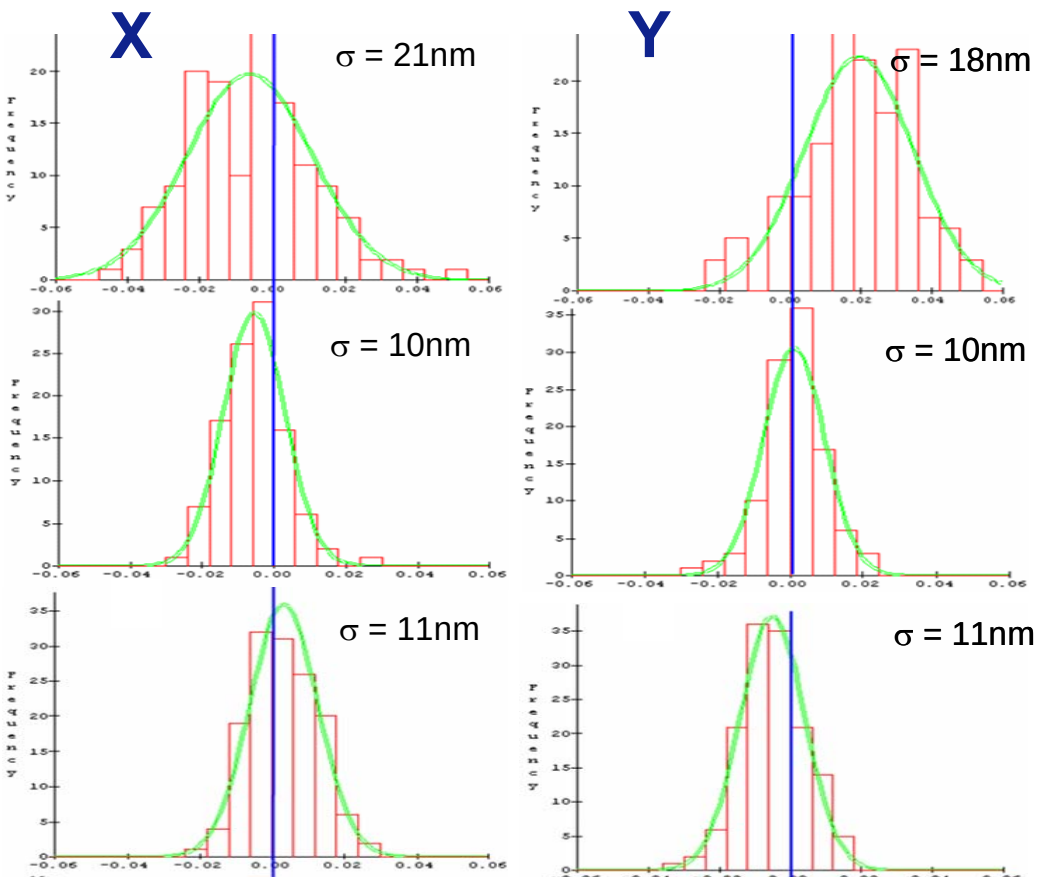
- Front-to-back Alignment on Glass Carriers

3 different alignment methods on PAS5500/700, compared in a CMOS 0.18um process, after Met1



Front-side TTL
(SPM Marks)

Front-side OA
(SPM Marks)

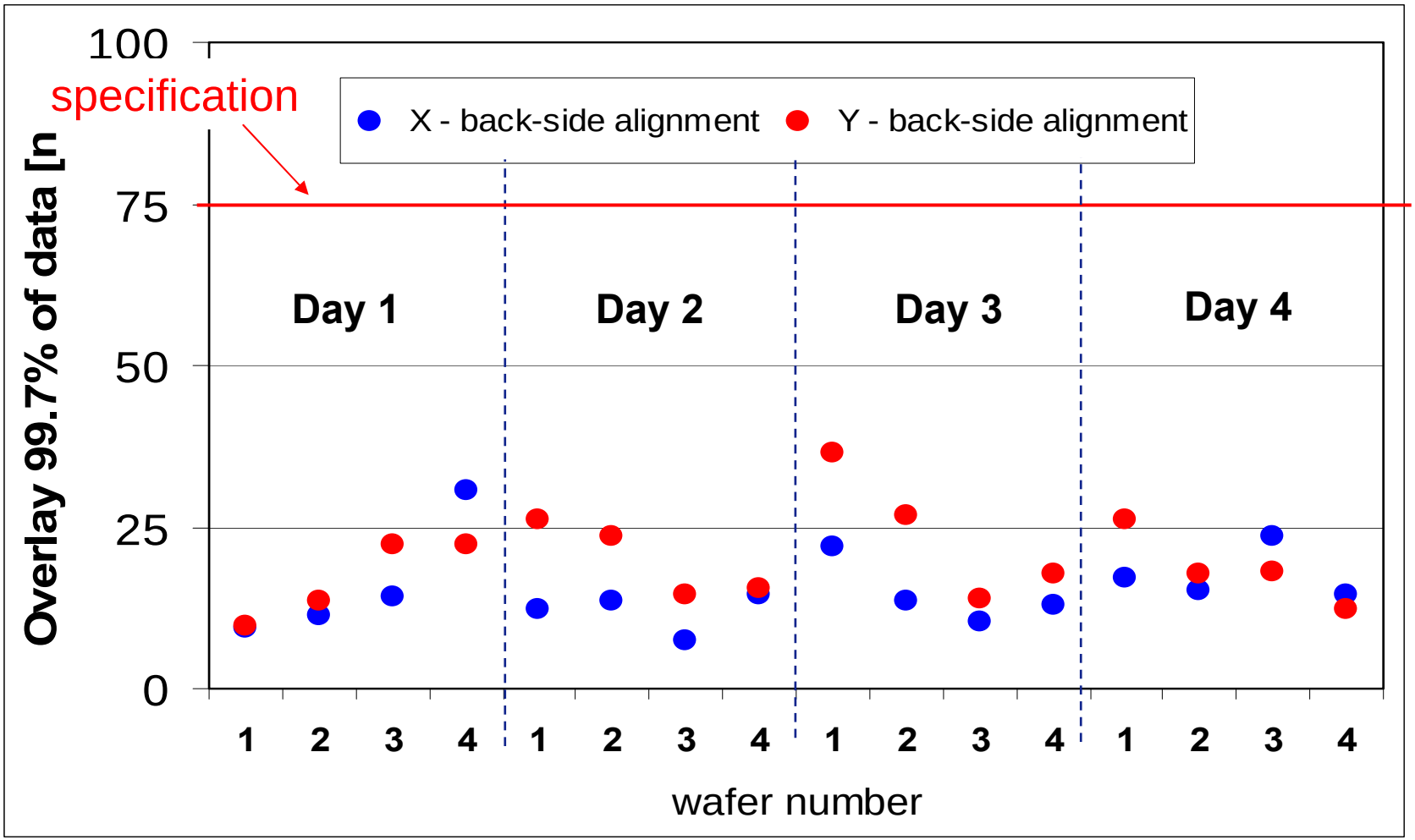
3DAlign™
Back-side TTL
(PM marks)

*** Mis-registration measured after process correction**
*** Box-in-box data from KLA5300**

- Both OA (Athena) and back-side TTL (3DAlign) outperform front-side TTL alignment, as shown by the overlay performance in a CMOS 0.18um process

PAS5500/275 stepper: Overlay Performance < 50nm
Using BTBA TTL

PAS5500/275



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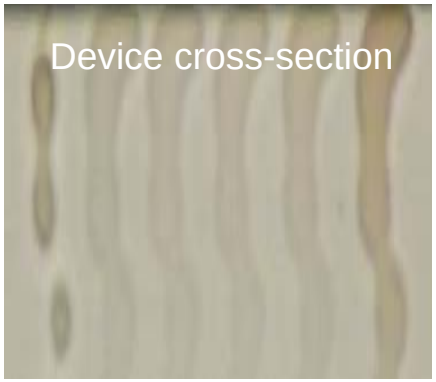
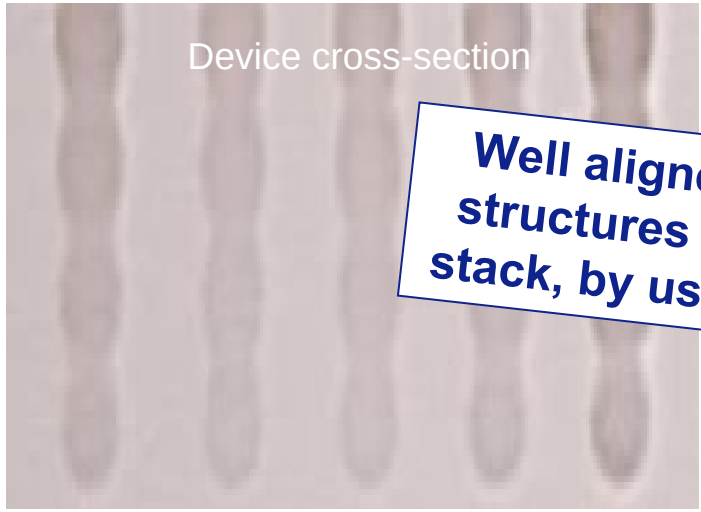
Successful alignment on the back-side and process on the front-side using 3DAlign™ BTBA



Misalignment in front-side alignment scheme



Well aligned junction structures in thick epi stack, by using 3DAlign

Cross-section of layer stack manufactured using the 3DAlign back-side alignment scheme

- Successfully introduced in power devices volume manufacturing:
  - Fab capacity for epi stack increased (+36%)
  - Cycle time for epi stack decreased (-26%)

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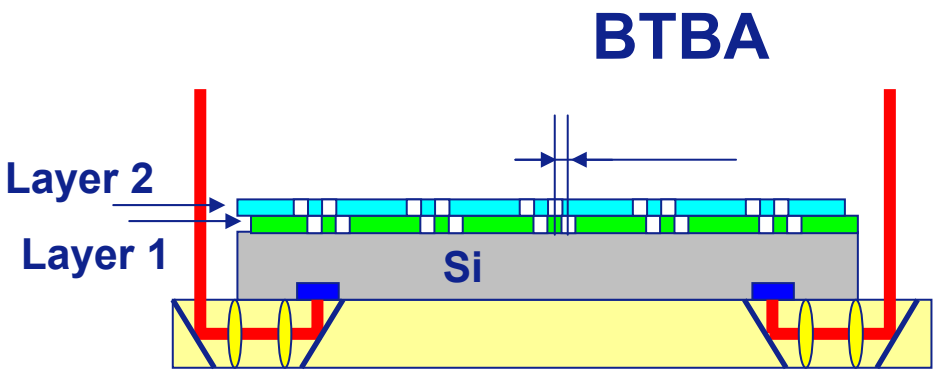
Requirement of smooth back-side surface for BTBA



Requires <u>smooth wafer back-side</u> to accommodate alignment marks

- As an efficient alternative to using DSP wafers, 2 experiments were conducted and overlay was measured on PAS5500/100:
  - Testing of back-side ground SSP wafers with different grits
  - Testing SSP wafers that received an additional back-side treatment

Ground SSP wafers with different grits can be used for back-side alignment

PAS5500/100

- Starting with SSP wafers, the wafers were “back-ground” using 1700, 2000, 4000 and 8000 grit; alignment and overlay were measured:

Grit	Avg Roughness (Angstrøms)	WQ* signal (%)	8.0-8.8 shift** (M1Bi1) (μm)	Backside Overlay (X, Y) (nm)
1700	637	44	-0.158, -0.218	33, 46
2000	613	44	-0.163, -0.224	24, 24
4000	337	45	-0.164, -0.220	40, 43
8000	290	63	-0.021, -0.054	20, 17

** : WQ signal strengths above 1% are typically sufficient for proper alignment (PAS5500).*

*** : Typically 8.0-8.8 shifts smaller than 0.25 μm ensure proper alignment.*

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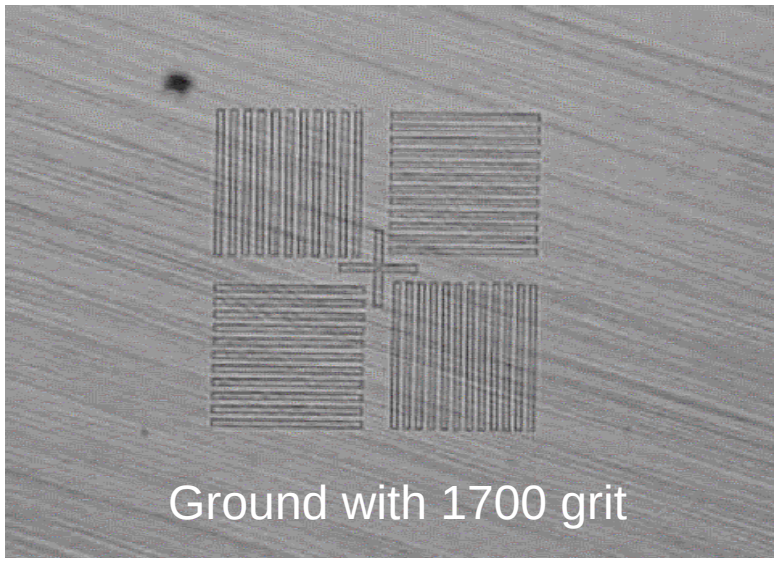
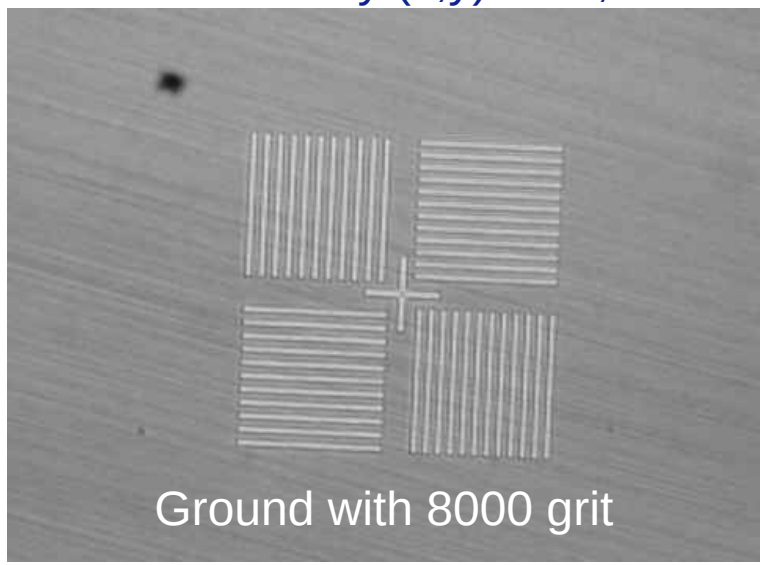
Ground SSP wafers with different grits can be used for back-side alignment

PAS5500/100

Backside Overlay (x,y) = 33,46 nm



Backside Overlay (x,y) = 20,17 nm

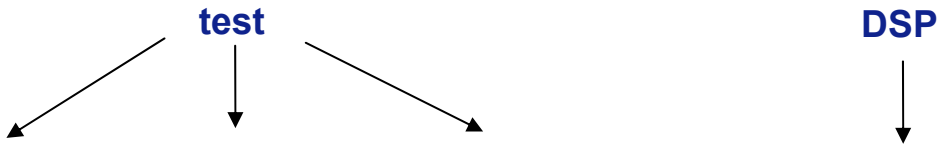


- Conclusion: Residual surface roughness up to 700 Å with standard marker depth allowed for backside alignment < 100nm on un-processed wafers

Back-side treated SSP wafers* can be used for back-side alignment

PAS5500/100

- Alignment reproducibility standard deviation (3σ); test wafers shows similar performance as reference DSP wafers



marker depth	855 nm		490 nm		150 nm		160 nm	
	test wafer 2		test wafer 3		test wafer 4		DSP wafer	
	X (nm)	Y (nm)	X (nm)	Y (nm)	X (nm)	Y (nm)	X (nm)	Y (nm)
W1 (FRONT)	1	2	2	1	2	1	2	2
W2 (FRONT)	1	2	2	2	2	2	3	3
B1 (BACK)	6	3	4	2	5	2	4	2
B2 (BACK)	4	3	4	4	4	3	4	3
B3 (BACK)	5	3	4	3	5	3	4	4
B4 (BACK)	4	3	5	3	4	2	5	4

** Supplied by MEMC*

Back-side treated SSP wafers* can be used for back-side alignment

PAS5500/100

- Overlay performance

Wafer ID	Markerdepth (nm)	back-side alignment measurements			
		Lowest WQ (%)	Highest Δ-shift (um)	MCC	overlay vector 99.7% (nm)
1	1200	0	0	0	na
2	855	14	0.143	0.95	44
3	490	14	0.198	0.93	38
4	150	10	-0.102	0.95	36

- Conclusion: With optimized marker depth, these SSP wafers (with an additional back-side treatment) provided 3DAlign BTBA overlay performance within specifications

** Supplied by MEMC*

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Conclusions – Alternatives for DSP

- Two alternatives for DSP wafers for use in a back-side alignment scheme have been successfully tested on non-processed wafers:
  - Back-side grinding of SSP wafers
  - Using pre-treated wafers supplied by MEMC*
- These alternatives can be cost-efficient compared with the use of DSP wafers if these wafers can be qualified in a production fab environment**

** Please consult directly your local MEMC contact, or contact mmaffe@memc.it or ldhollander@memc.it for more details*

*** Qualification of these alternative method(s) in a production environment has not been part of this study by ASML*

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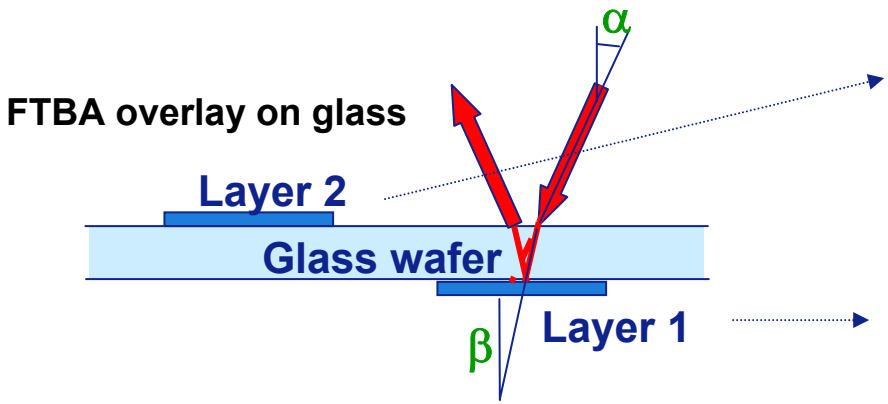
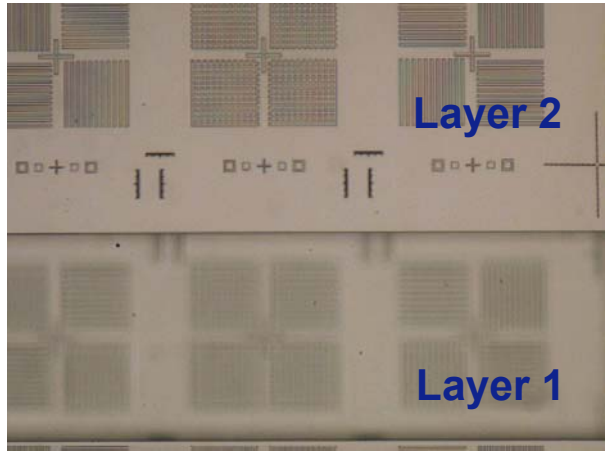
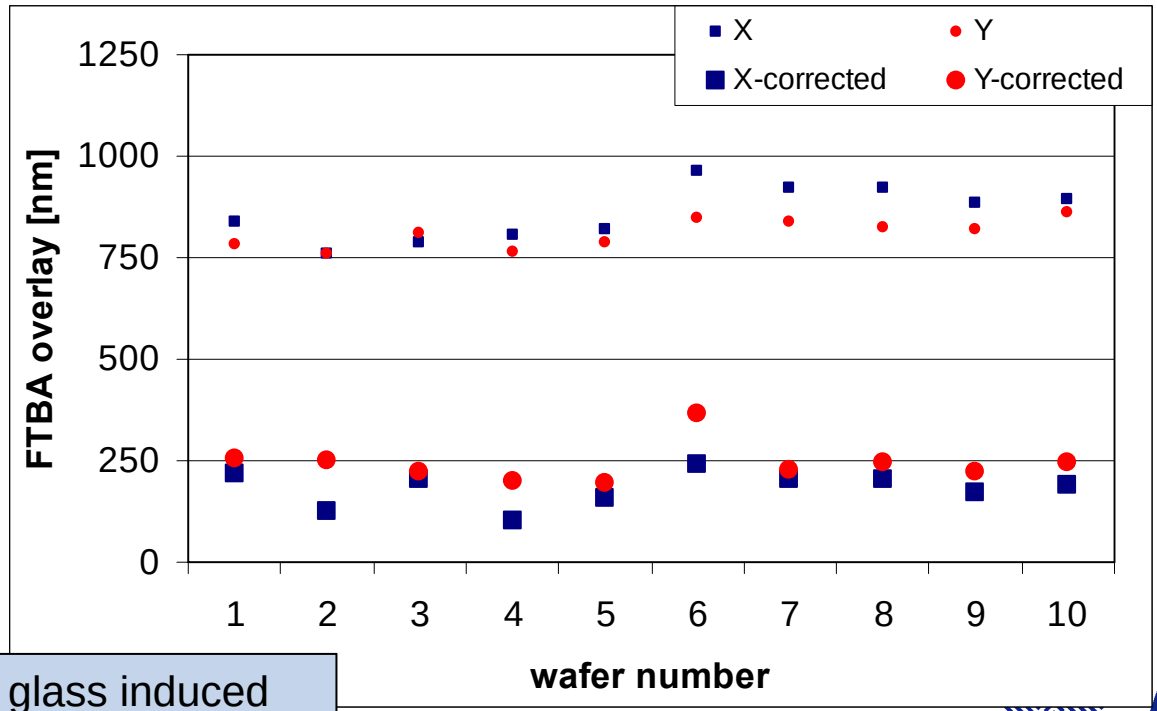
- Front-to-back Alignment on Glass Carriers

Stable Front-to-Back Alignment on PAS5500

Double sided processing







→ Corrected for glass induced translation error (~ 600nm)

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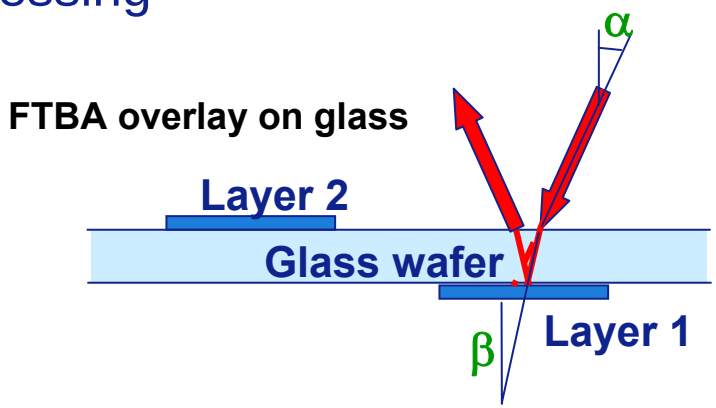
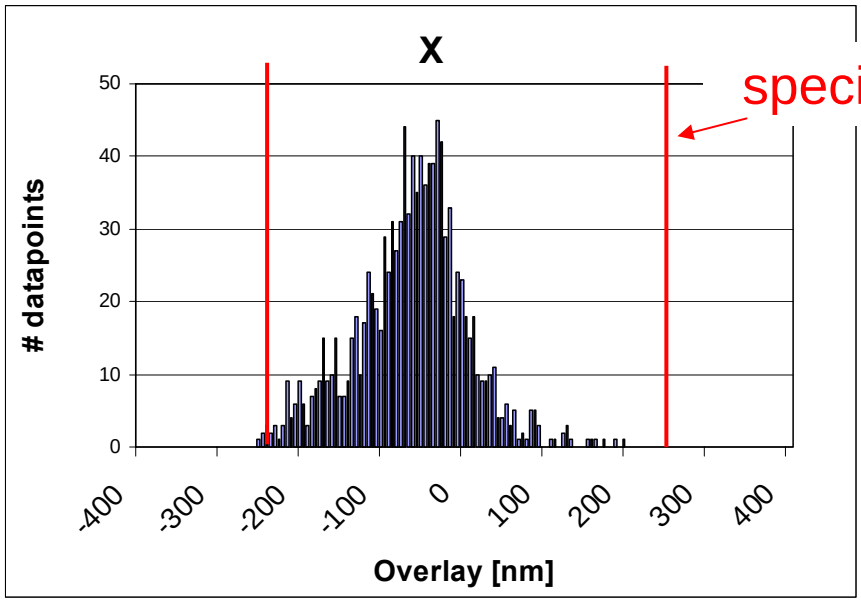
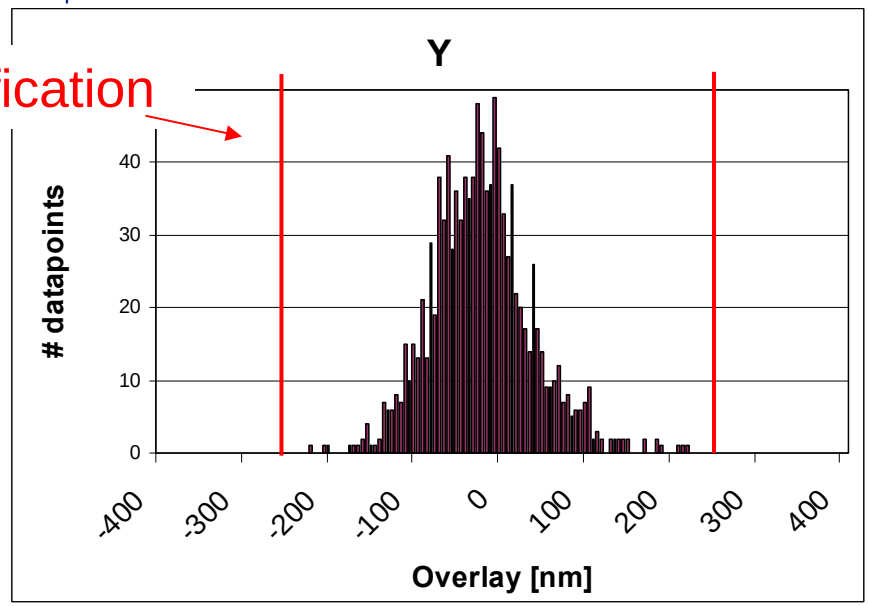
Front-to-Back Alignment on PAS5500: 3σ < 250 nm

Double sided processing



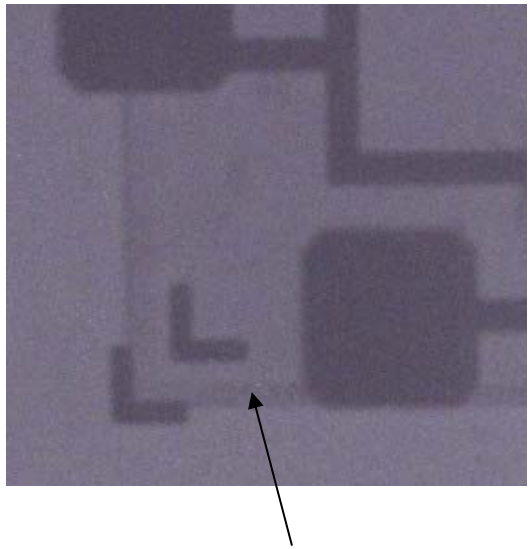


specification

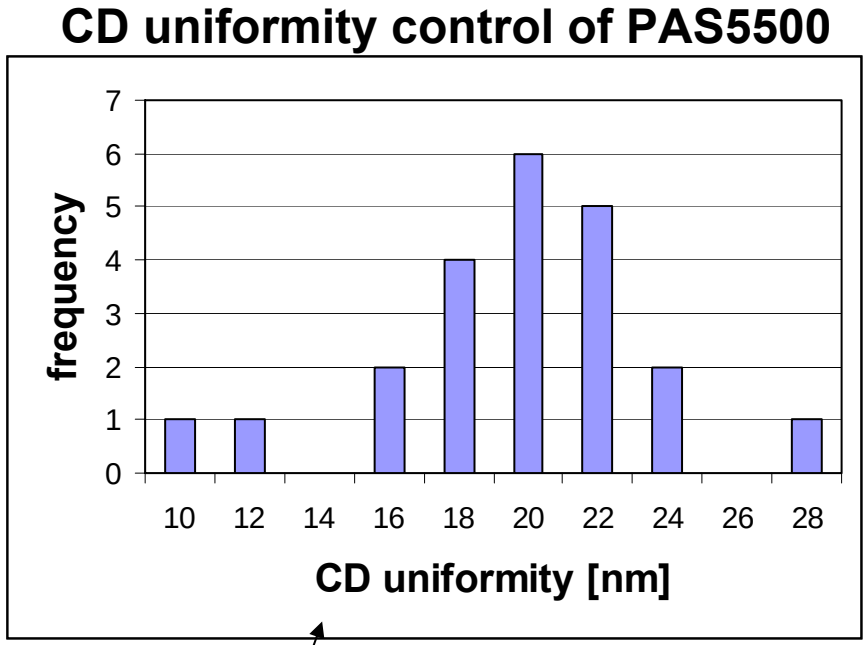


→ Glass induced error measured and corrected, but still containing (correctable) errors

Manufacturing smaller and more sensitive pressure sensors



IR picture: well-aligned backside cavity of pressure sensor



Good CD control of piezoresistive elements of P-sensor

- Smaller and more sensitive pressure sensors possible by:
  - Deep submicron double side alignment overlay
  - Excellent CD control of reduction lithography tool

Overview

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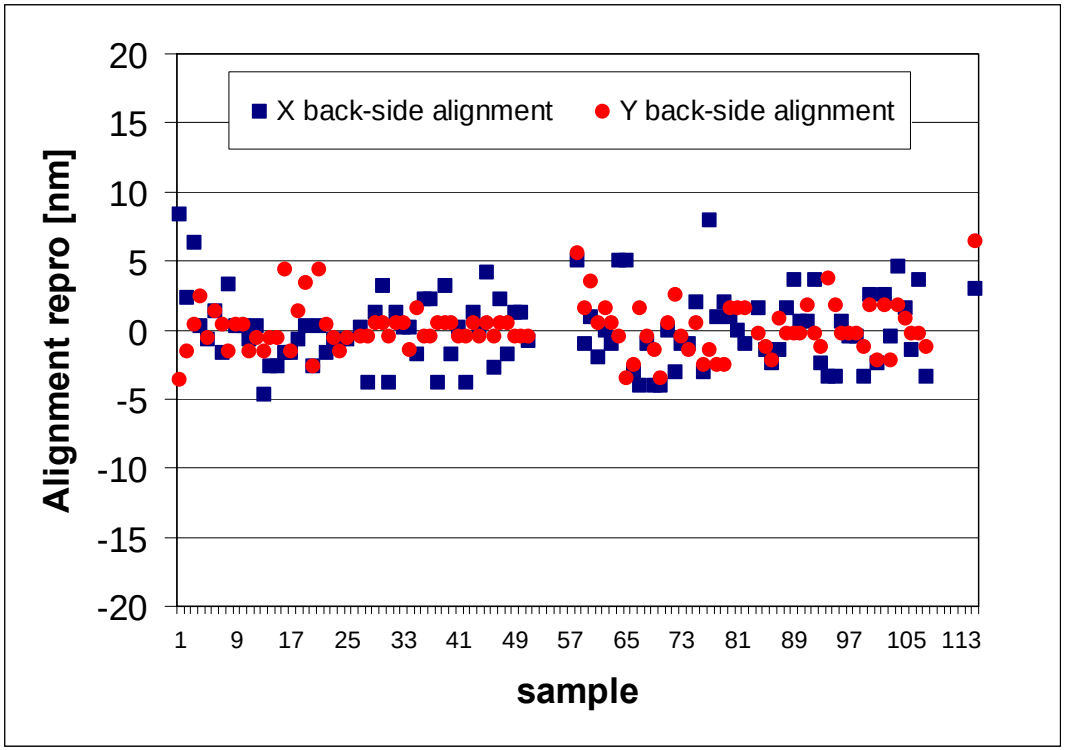
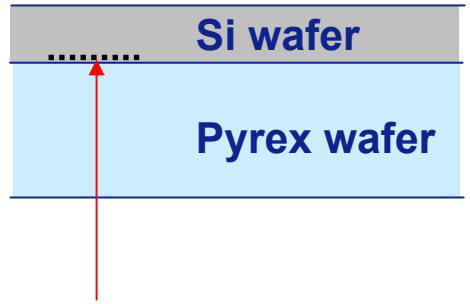
Alignment repro through glass gives stable signal



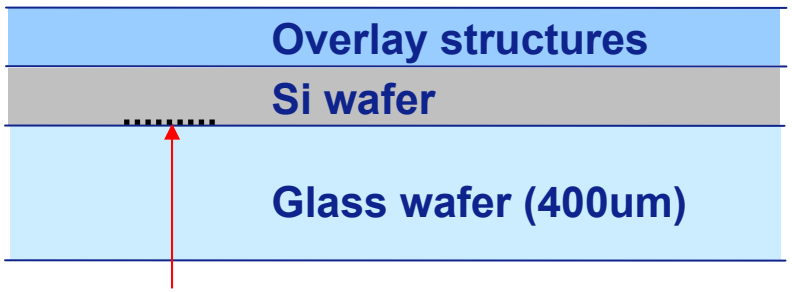


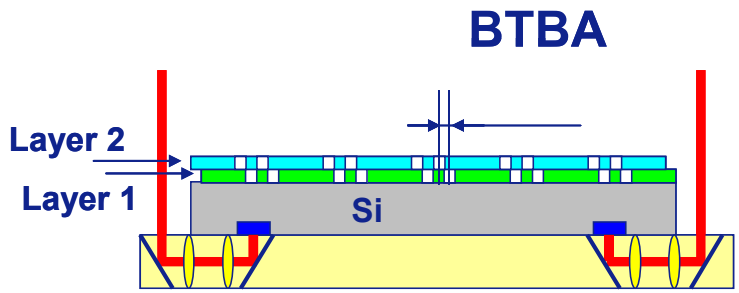
- Back-side alignment reproducibility through a pyrex carrier for 2 alignment marks (about 50 measurements per mark)

BTBA overlay on PAS5500/100 – Si on glass is well within design rules for CMOS IS TSV's*

Overlay [nm] (99.7% of data)	BTBA Ov without glass carrier	BTBA Ov with glass carrier
X	28	274
Y	31	289

CMOS IS application for microbump, RDL and passives processes





** TSV = Through Si Via for interconnect manufacturing*

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Conclusions

- Back-side alignment performance (BTBA) approaches standard front-side alignment; under process conditions *BTBA can be the better choice*
- Back-side alignment provides a very cost-efficient alternative alignment scheme by *decoupling process from alignment* (fewer process layers)
- New methods for further *driving down substrate costs* of a back-side alignment scheme are presented
- Double side alignment (FTBA) application of 3DAlign provides *deep sub-micron overlay performance*, required for volume manufacturing of advanced MEMS, Through Si Via for CMOS IS and stacked memory-logic, etc.

Thank you for your attention