“Enabling Semiconductor Innovation and Growth”

EUV lithography drives Moore’s law well into the next decade

BAML 2018 APAC TMT Conference
Taipei, Taiwan

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Vice President IR - Asia IR

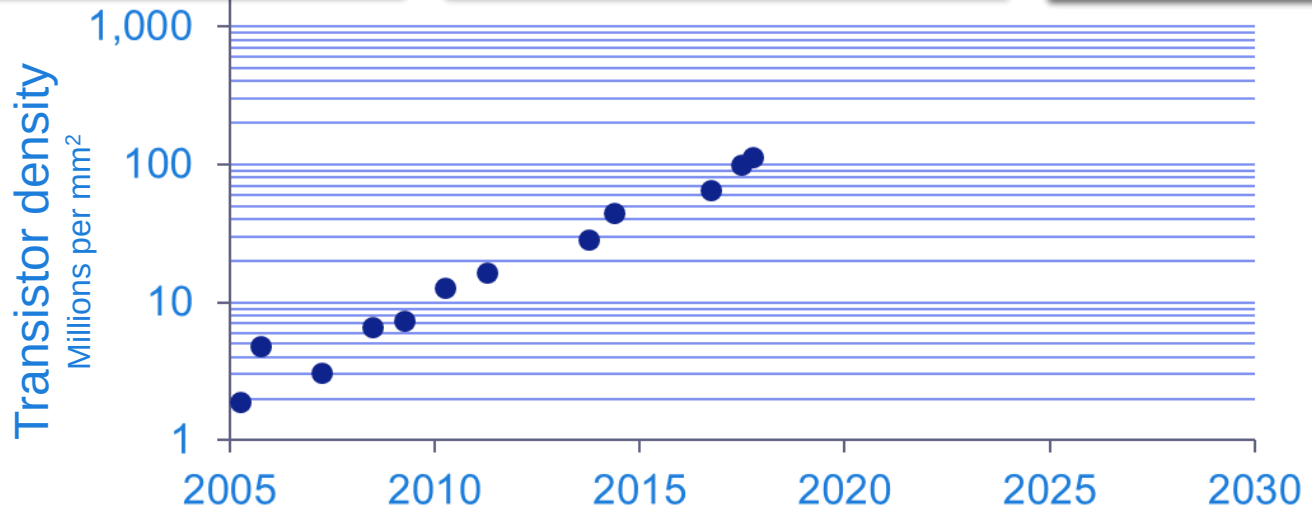
March 14, 2018

Forward looking statements

This document contains statements relating to certain projections, business trends and other matters that are forward-looking, including statements with respect to expected trends and outlook, including expected trends in the semiconductor market, expected annual operating profit, systems backlog, statements with respect to expected revenue growth in the semiconductor market, including expected forecast growth by market, the expected relative semiconductor content in automotive innovations by 2030, expected growth drivers in lithography demand in 2020, statements with respect to industry shrink roadmaps, EUV insertion plans and customer roadmaps, statements with respect to the expected continuation of scaling and transistor density by 2030, expectations with respect to EUV, including expected benefits, including lithography cost reduction and the expected benefits of High NA, target performance, EUV industrialization, including availability and throughput, shipments and the expectation that the installed base of EUV systems will double in 2018, the expected innovation pipeline in the next 10 years and beyond, the expected increased impact of new scalable memory types in the next 10 years and the expectation that such types will continue driving lithography, statements with respect to shrink being a key driver supporting innovation and providing long-term industry growth, lithography enabling affordable shrink and delivering value to customers, and statements with respect to the expected continuation of Moore's law and that EUV and scaling and shrinking will continue to support and enable Moore’s law and drive long term value for ASML beyond the next decade. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "targets", "commits to secure" and variations of these words or comparable words.

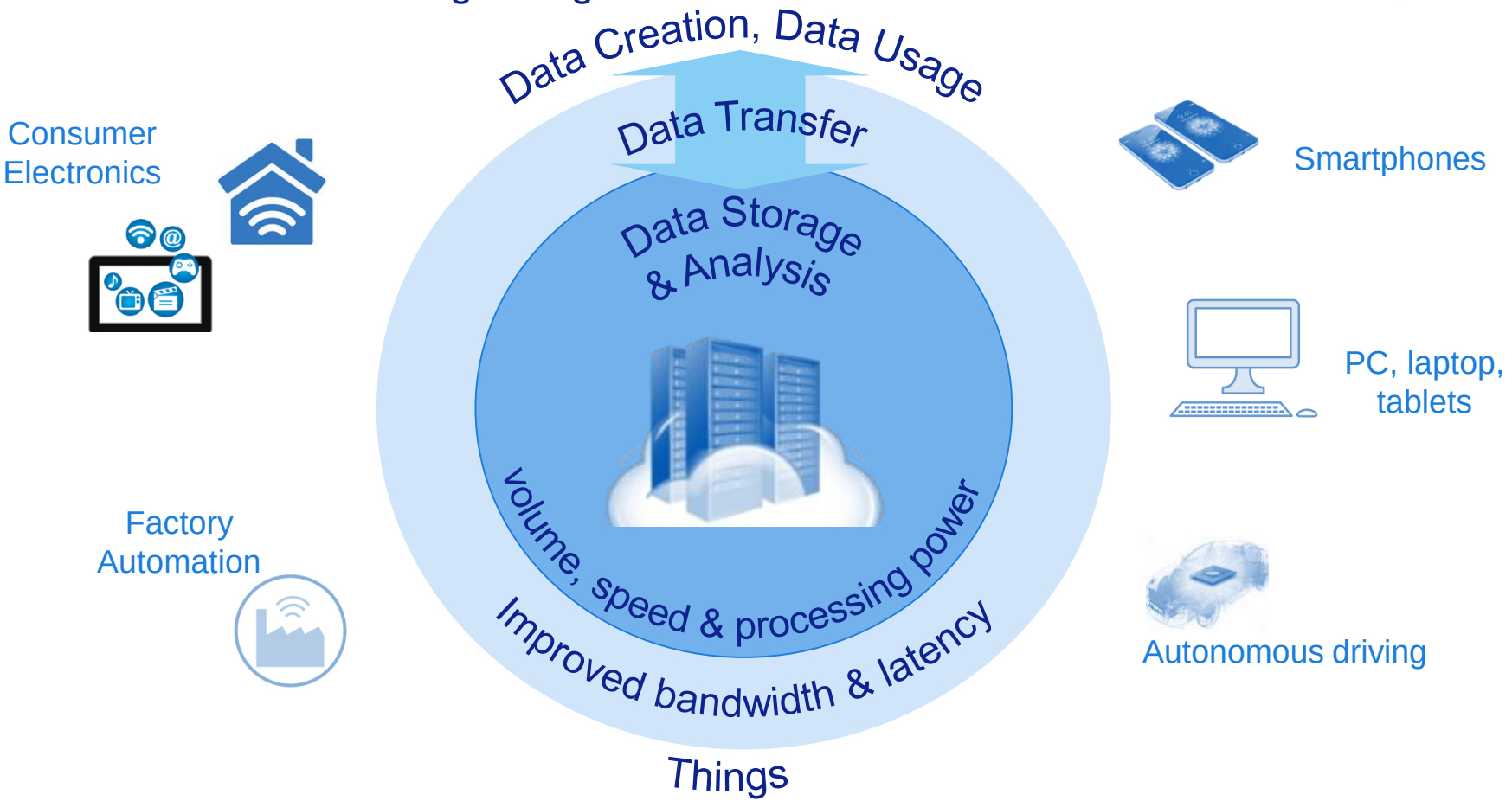
These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products including EUV, the number and timing of EUV systems expected to be shipped and recognized in revenue, delays in EUV systems production and development and volume production by customers, including meeting development requirements for volume production, demand for EUV systems being sufficient to result in utilization of EUV facilities in which ASML has made significant investments, our ability to enforce patents and protect intellectual property rights, the outcome of intellectual property litigation, availability of raw materials, critical manufacturing equipment and qualified employees, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases, results of the new share repurchase plan and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Semiconductor Scaling has changed how we…



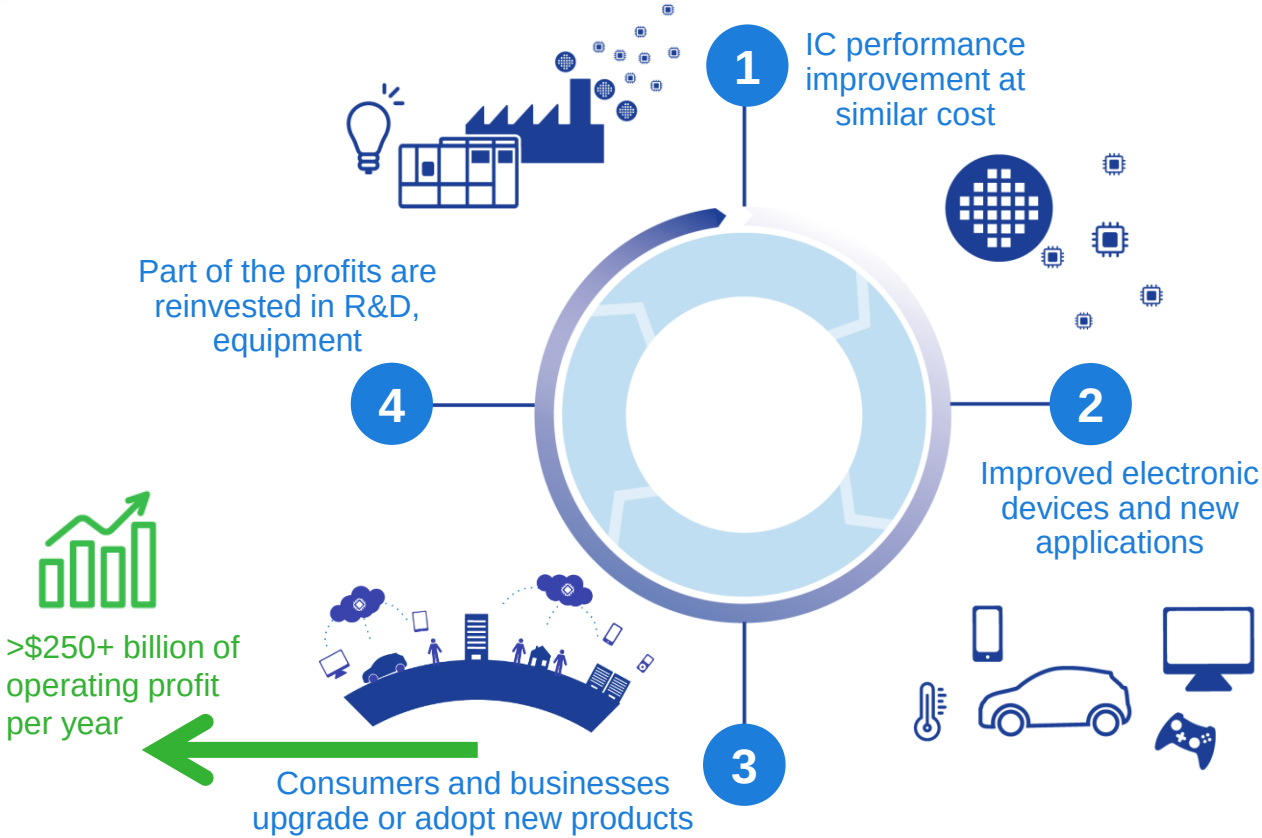
Insatiable need to transfer, store and analyse data

drives a continuous and growing demand for semiconductors



Scaling/Shrinking Supports Moore's Law

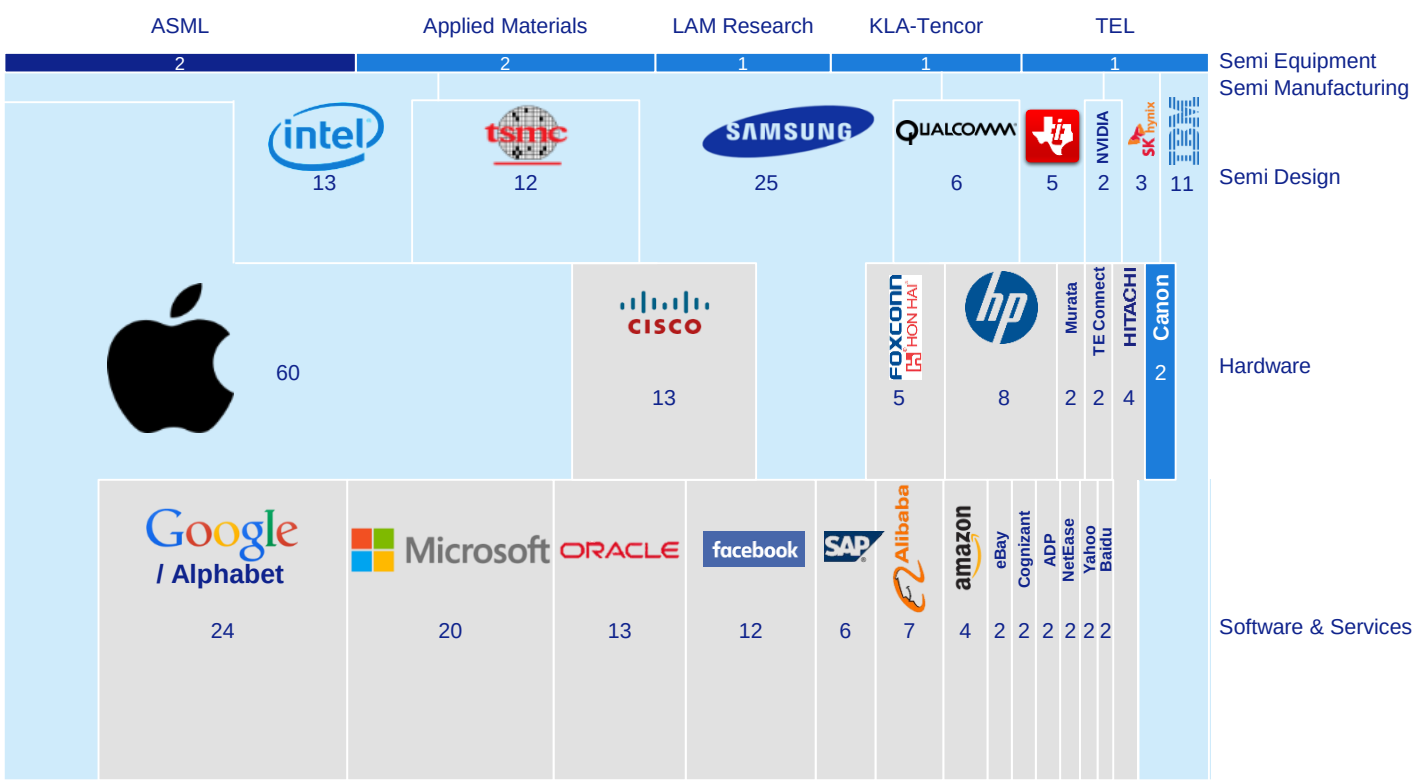
Moore's Law is underpinning a business model

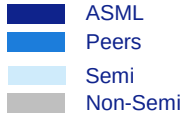


Takeaways

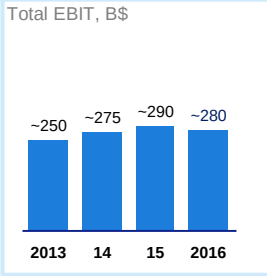
>$250+ billion of annual operating profit is riding on the industry's ability to keep this cycle going

ASML operates in a highly profitable value chain with strong incentives to compete and drive innovation





There remains a lot of income generated

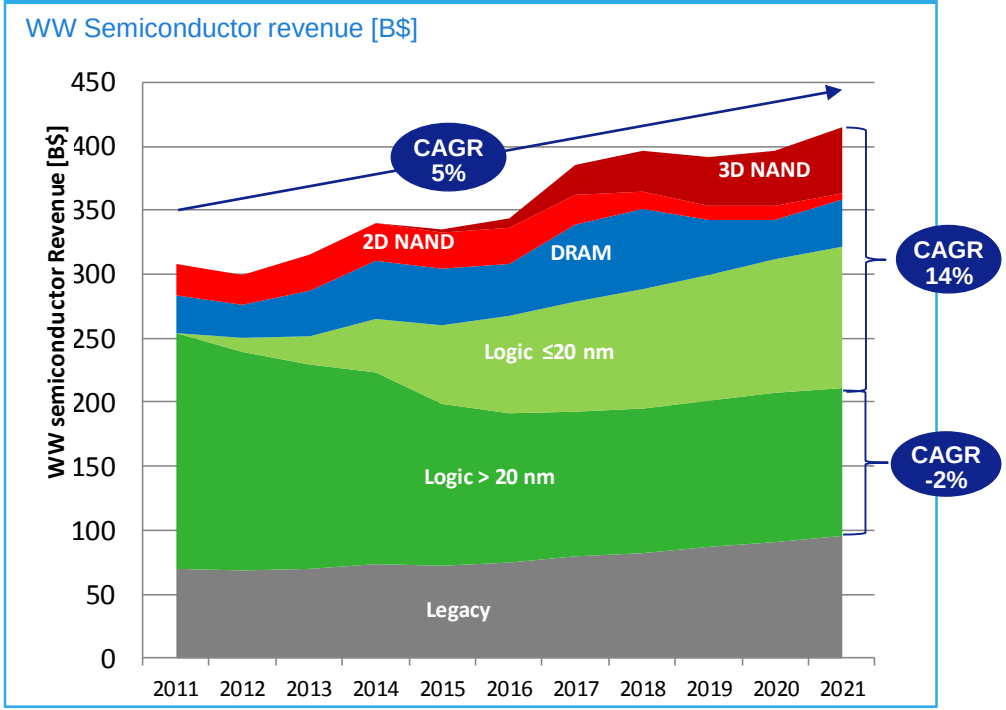


Top technology companies in our ecosystem (EBIT CY2016, B$)

Source: Bloomberg (GICS 45 classification)

Leading edge Logic and Memory processes drive growth in semiconductor markets

Revenue growth is coming from those segments where roadmap innovation continues: advanced logic, DRAM and NAND (non-volatile memory)



Source: ASML analysis, Gartner

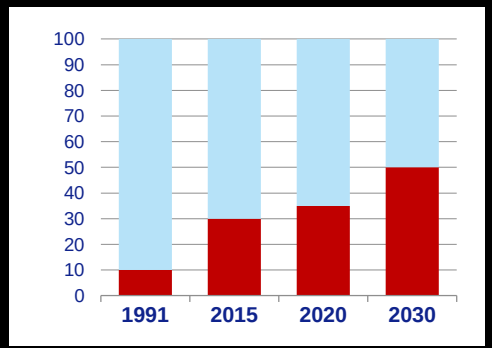
Lately we've seen the following trends in semiconductor markets:

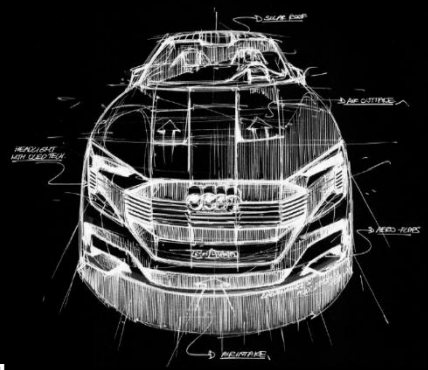
- Strong transition to 3D-NAND to continue enabling large capacities at lower cost
- Slowing DRAM roadmap leading to lower bit growth resulting in price increases, triggering capacity investments
- Increasing focus on new memory devices (i.e. x-Point)
- Continuing strong drive for logic shrink with process improvements coming on an annual cadence

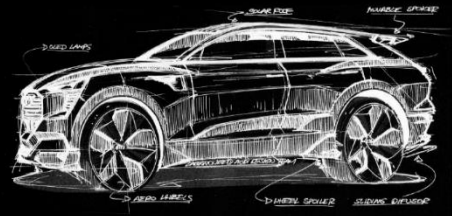
Semiconductors drive 80% of automotive innovations

Expected to represent 50% of the cost of goods in 2030 (per Audi)

Relative Semiconductor content in automotive [%COG]







80%

of all **innovations**

are directly or indirectly

enabled by semiconductors

Source: Berthold Hellenhtal, Audi, “Cross industry collaboration networks accelerate innovations”, ISS Europe, Munich, March 2017

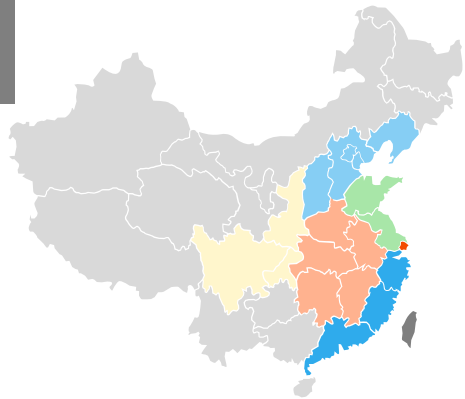
Disruptive trends also drive litho demand

Growth drivers: 2017 to 2020+

NAND — Storage Class Memory Growth and transition to 3D NAND

Source: John Kelly III, IBM, December 2015

CHINA — China Greenfield Investments

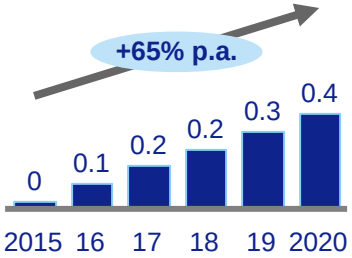


Chinese government supports massive investment into domestic semi industry

IoT — Emerging connected devices market (IoT)

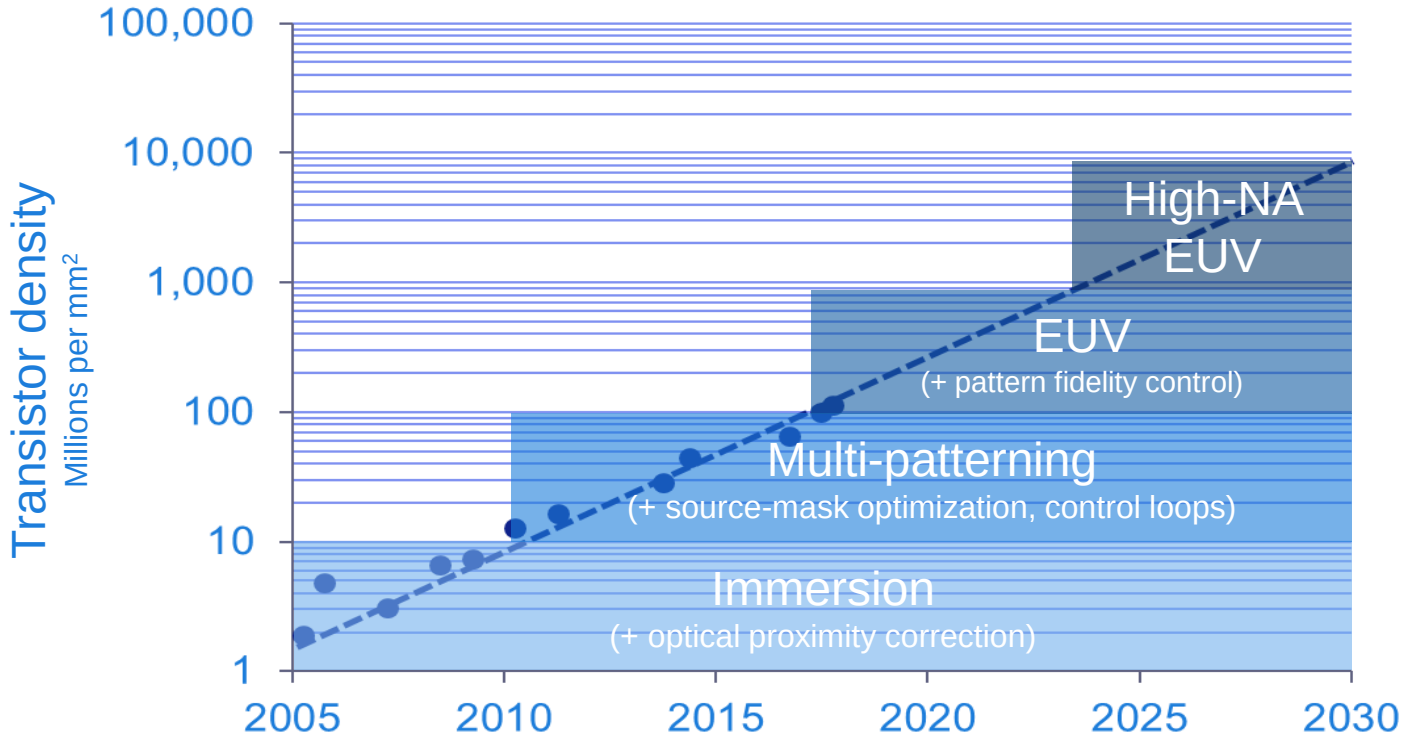
Internet of Things will connect a growing number of devices from 12 billion in 2012 to **50 billion in 2020**

IoT devices shipments, B units



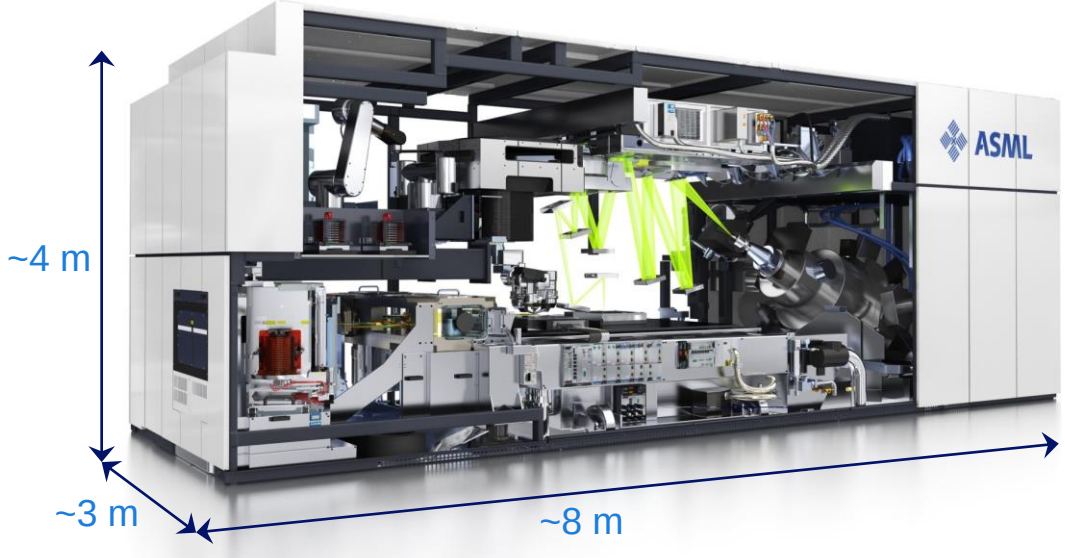
Scaling will continue towards 1 billion transistors per mm^2

We are ready to support the Semi industry's ambition through the extension of Moore's Law



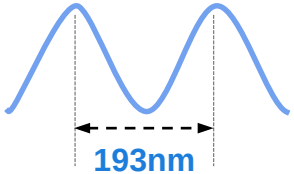
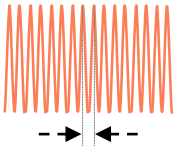
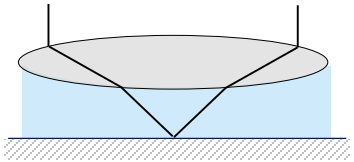
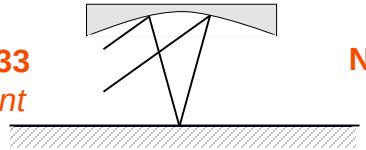
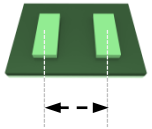
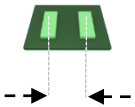
EUV – A New Technology in Lithography

- New technology transitions: customer perspective
- EUV progress & plans
- EUV infrastructure
- EUV extendibility



What is EUV? A litho technology that delivers 3x -> 5x Resolution Enhancement

Resolution = k_1 x $\frac{\lambda}{NA}$

	ArF immersion	EUV
k_1 difficulty, limit = 0.25	**k_1 = 0.265** strong OPC mask	**k_1 = 0.32** OPC mask
λ Wavelength		
NA Numerical Aperture	**NA 1.35** *Maximum* 	**NA 0.33** *Current*  **NA > 0.5** *Future*
Resolution Minimum pitch	 **76nm** *38nm half pitch*	 **26nm** *13nm half pitch*	 **< 16nm** *< 8nm half pitch*

Dilemmas when adopting a game-changing technology
Early decision making

	It works	It does not work
We have it		
We do not have it		

How customers approach new technology insertions

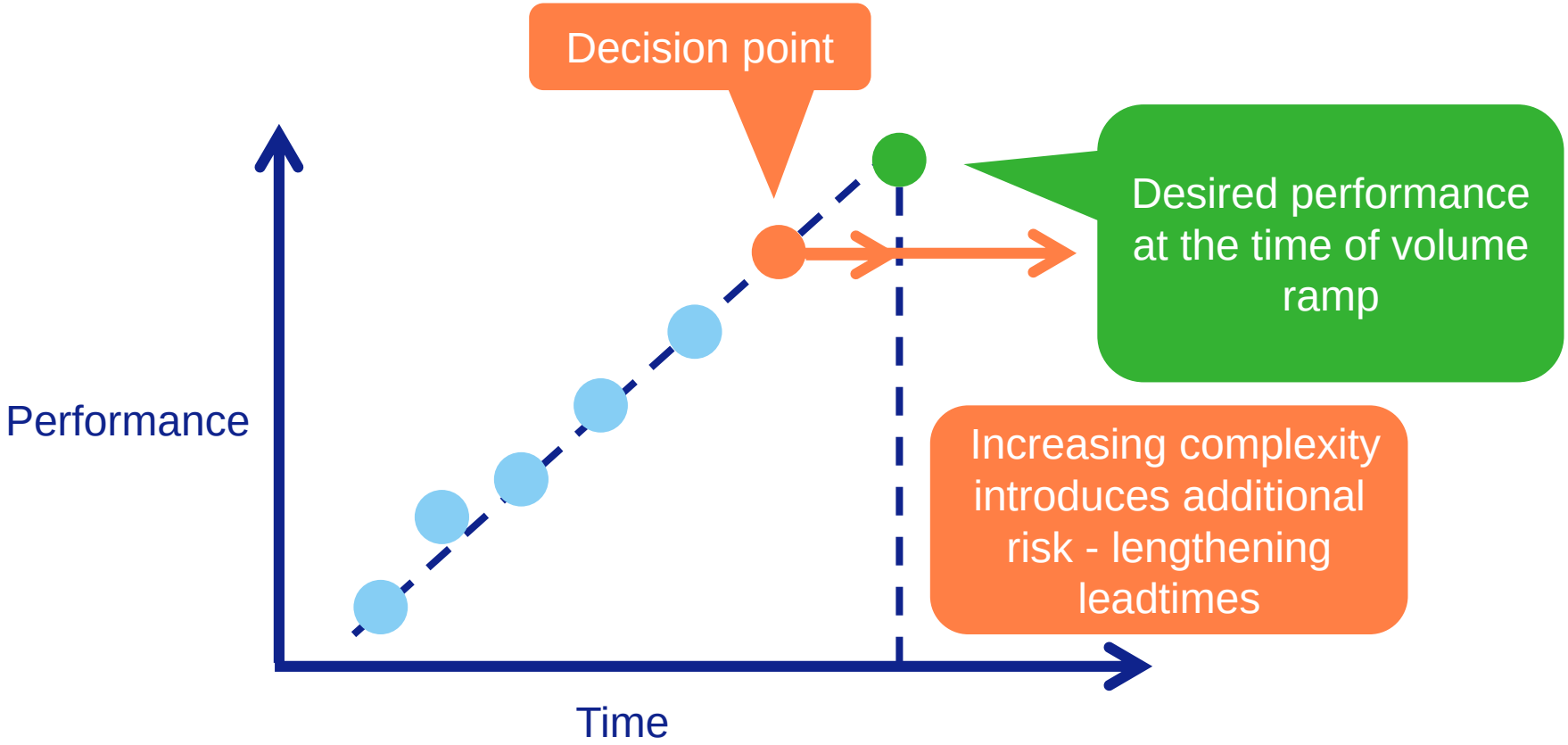
- Visionary/champion
- R&D enthusiasm
- First results
- Business manager “Shouldn’t we go for this?”
- Manufacturing push back
- Tough criteria, entrance hurdles
- Dynamics: progress vs. milestones
- Product roadmap timing
- Business decision with up/down ticks
- Different risk appetite per customer and per segment

EUV Case

- Done
- To be addressed
- To be considered

Technology transitions: decisions based on early results

“You have to move to where the puck will be, not where it is” (Wayne Gretzky)

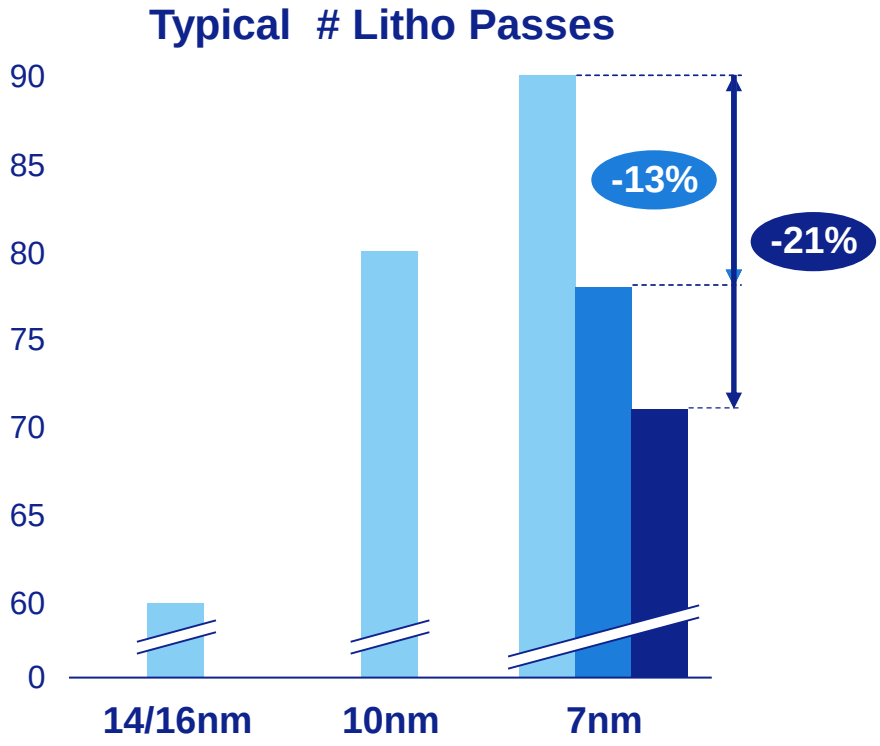


General rule of New Technology adoption

Early adoption is risky

Late adoption is expensive

EUV “rewards” at 7nm are clear: simpler process, shorter cycle time enabling faster yield ramp and time to market



Cycle Time Advantage

	Optical	EUV
No. of critical masking steps	30	10

30 day reduced cycle time @
1.5 days per masking level

- Cycle time reduction in development
- Cycle time reduction in manufacturing

Yield & Quality Advantage

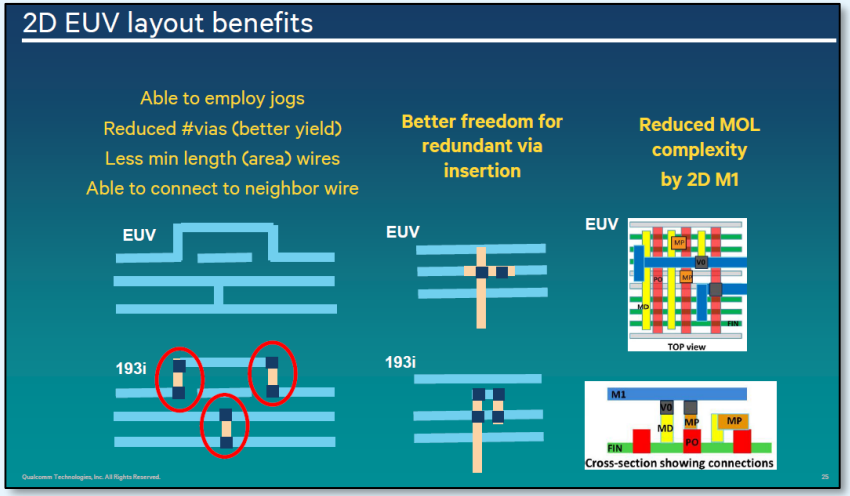
- Less variation in electrical parameter
- Tighter process control

Dr. Gary Patton, Global Foundries
SEMI ISS 2017

EUV introduction delivers compelling benefits in layout flexibility and process simplification

2D EUV patterning

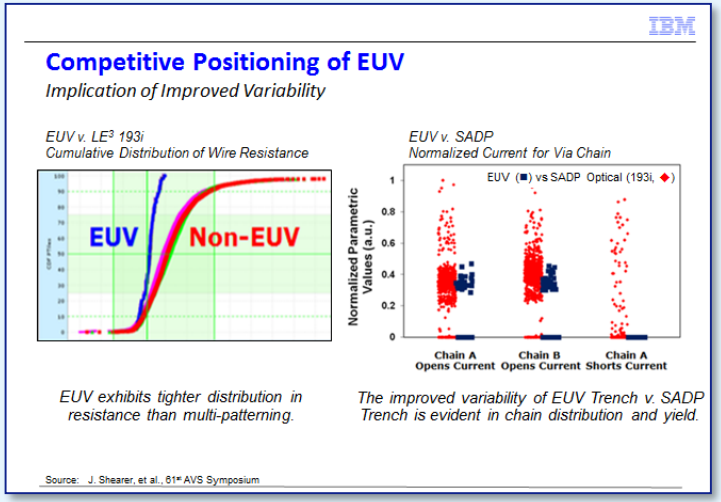
- More layout flexibility for designers
- Simpler process integration for engineers



Esin Terzioglu, Qualcomm, International Symposium on EUV, October, 2014

EUV process simplification

- Superior device performance
- Improved device variability

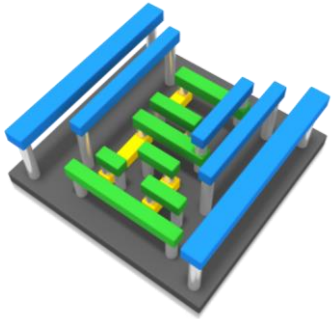


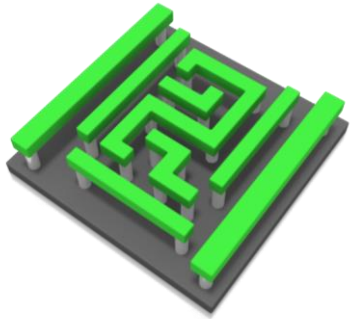
Jeffrey Shearer et al, IBM, AVS, November 2014

Resulting in more effective shrink + higher yields

EUV alternatives are very costly and complex

Immersion Multiple Patterning | **EUV**





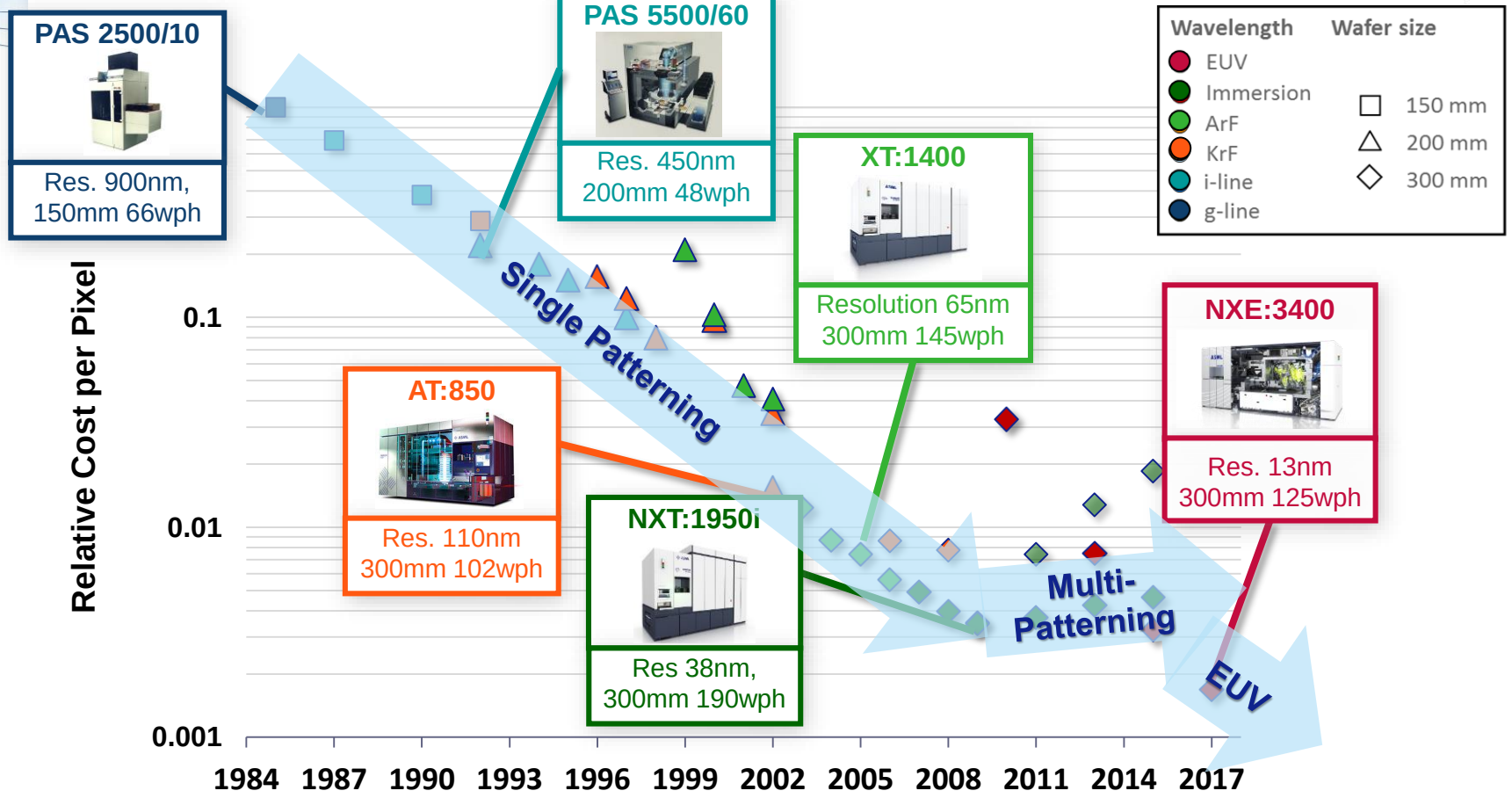
Process Steps
- CMP
- Dry Etch
- Metrology
- Lithography
- Track
- Deposition
- Clean
- Hard mask

LE3 = 3x Litho-Etch, “Triple patterning”

LE4 = 4x Litho-Etch, “Quad patterning”

SAQP = Spacer Assisted Quad Patterning
Cut = Separate Litho-Etch step

EUV enables continued Litho cost reduction



So where are we now?

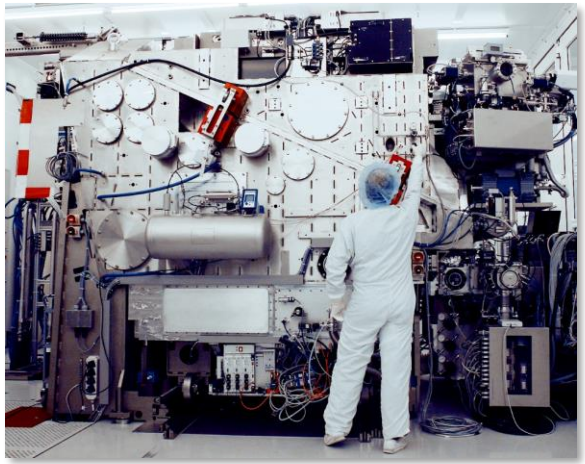
EUV industrialisation: from technology demonstration to HVM System

2006

ASML ships world's first EUV tool

Mark LaPedus
8/28/2006 09:00 PM EDT

EE Times



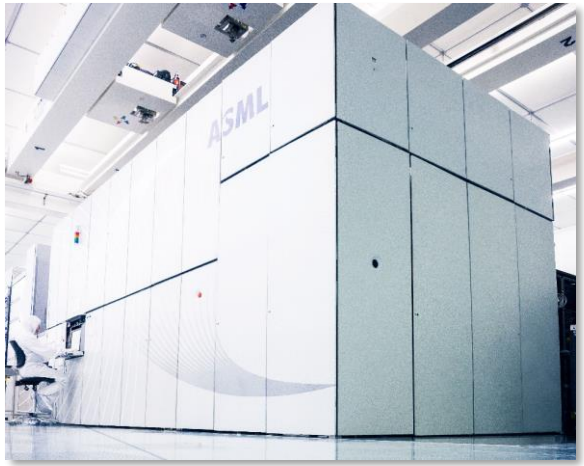
2017

ASML Revs EUV Engines

3400B and follow-on debut at SPIE

Rick Merritt
3/1/2017 10:20 AM EST

EE Times

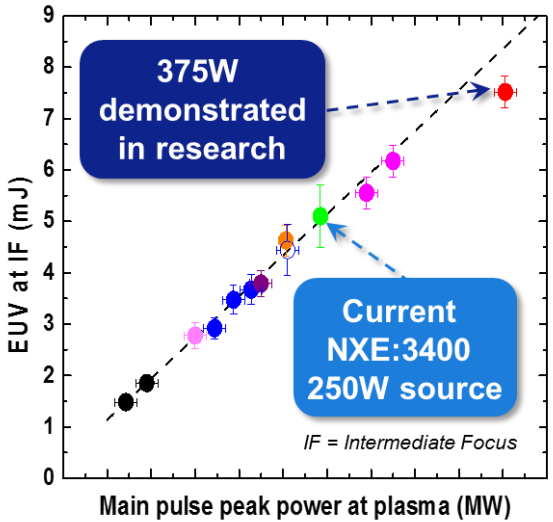


Resolution :	**40 nm**	**3x**	**13 nm**
Overlay :	**15 nm**	**10x**	**1.5 nm**
Throughput :	**0.05 WPH**	**2,500x**	**125 WPH**

Significant progress in EUV industrialisation

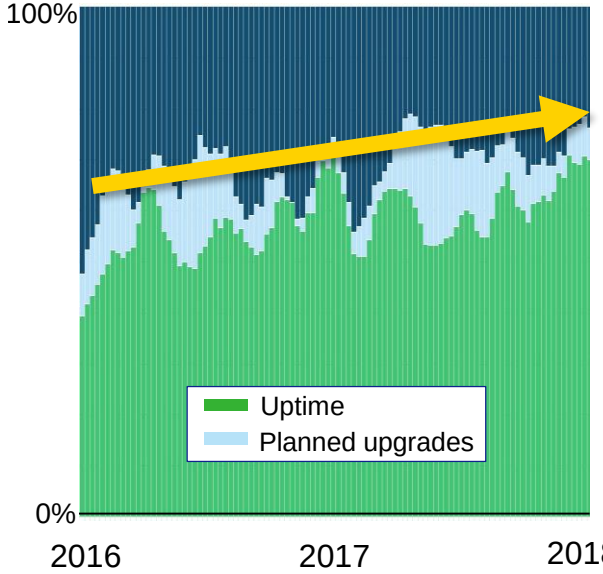
EUV Source & Throughput

Proven Power[1] & Wafers/Hour[2]



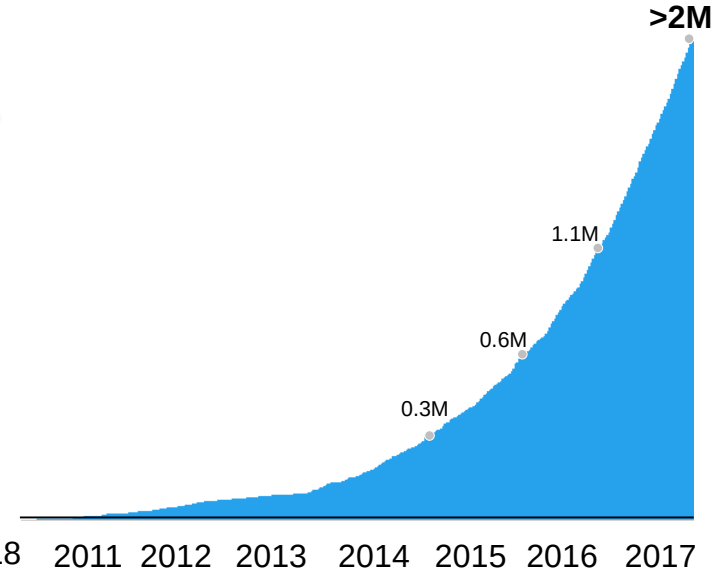
EUV Availability

Uptime %



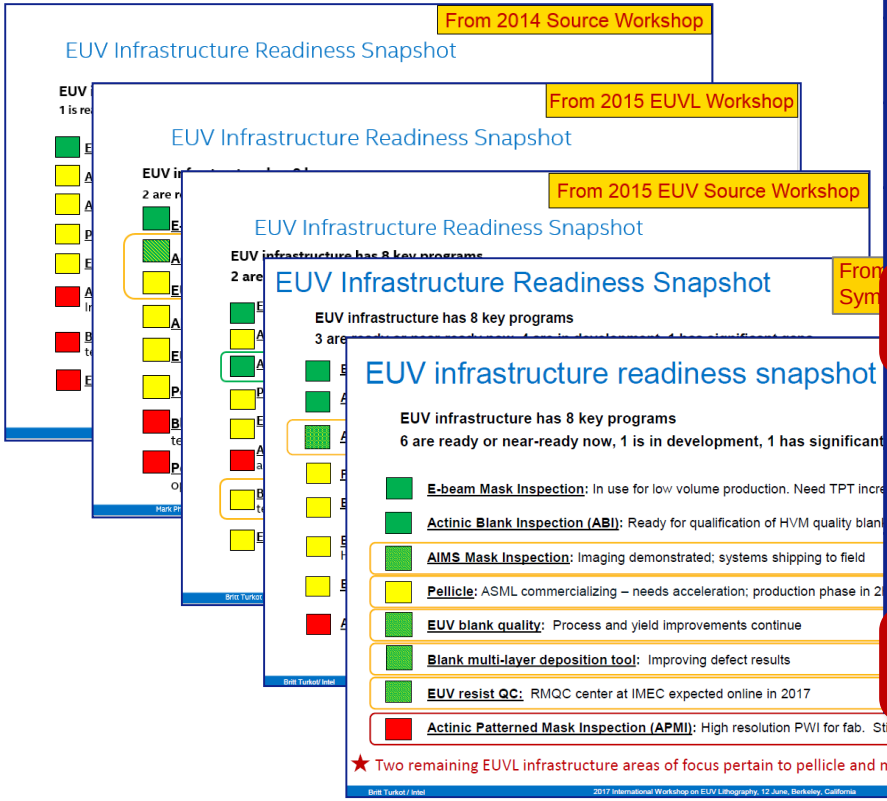
Cumulative EUV wafer exposures

NXE:3xxx, Wafers



[1] *Demonstrated on test rig,* [2] *Demonstrated at ASML or Customer,* [3] *Enables 145W/Hr on NXE:3400B*

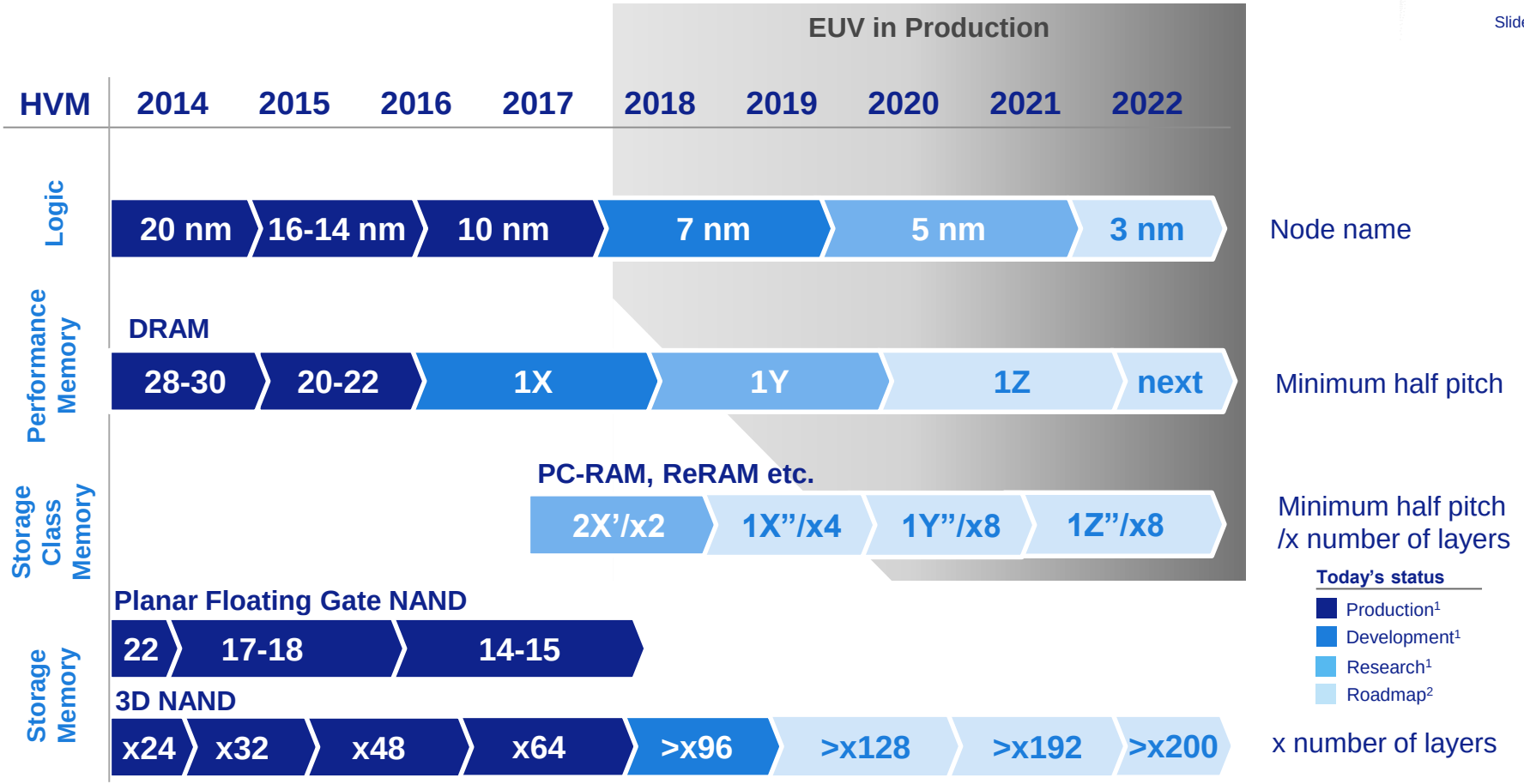
Evolution of EUV Infrastructure readiness



EUV Infrastructure	11/14	10/15	11/15	10/16	02/17
E-beam mask inspection					
AIMS Mask Inspection					
Actinic Blank Inspection					
EUV Pellicle					
EUV Blank Quality					
Blank multi-layer deposition tool					
EUV Resist QC					
Actinic Patterned Mask Inspection					

Source: Britt Turkot, Intel, International Workshop on EUV Lithography, California, June 2017.

Industry shrink roadmap and EUV insertion plans



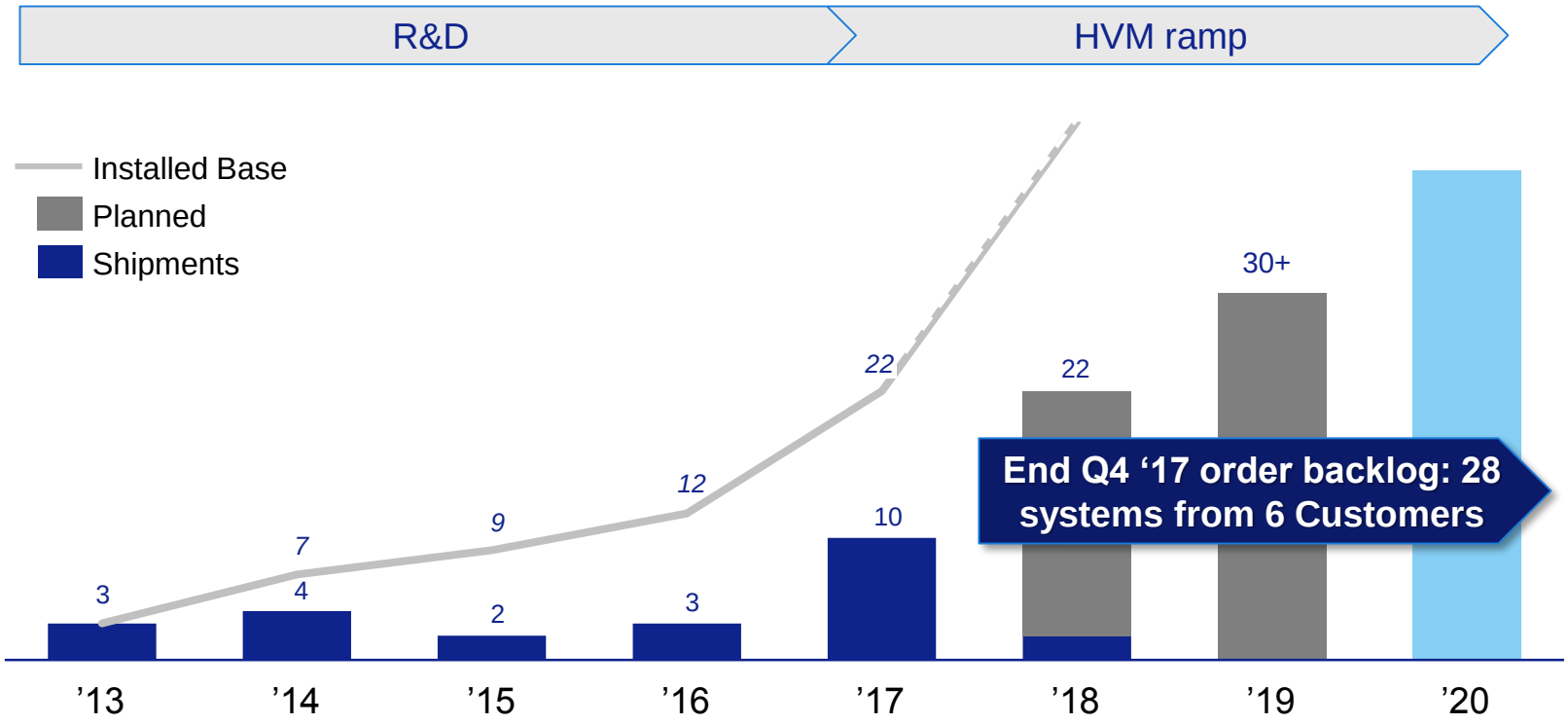
Source: 1) Customers - public statements,, IC Knowledge LLC; 2) ASML extrapolations

...which is supported by Customer shipments and orders

Installed Base of EUV systems expected to double in 2018

NXE:33x0 and NXE:3400

Shipments and Installed Base



And by recent customer statements on EUV insertion

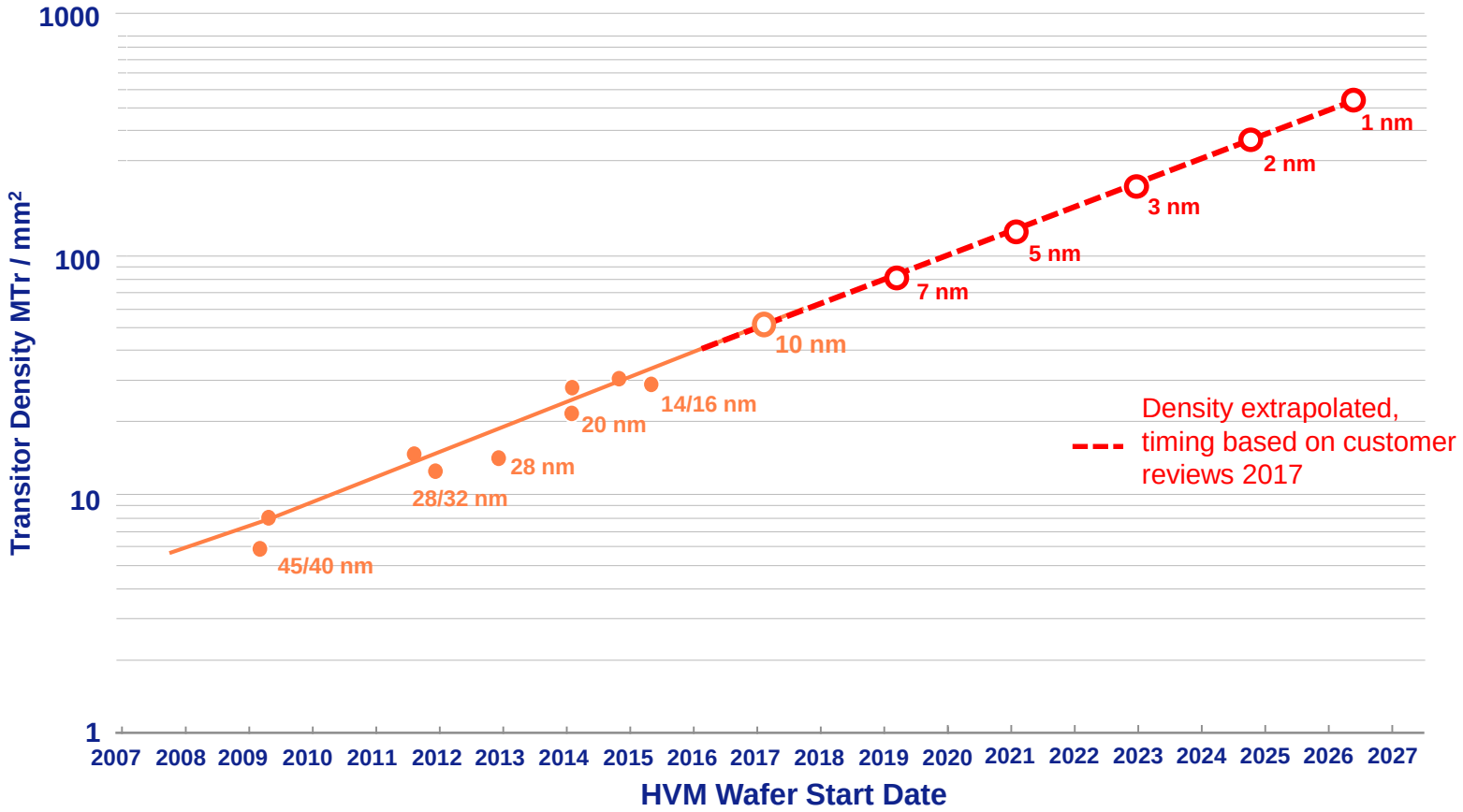
Mark Liu @ Q417 Earnings (Jan 2018)
"We are confident that our EUV technology will be ready for high-volume production for N7+ in 2019 and N5 in 2020."

Ho-Kyu Kang @ SEMICON Korea (Feb 2018)
"EUV will soon be in high volume production."

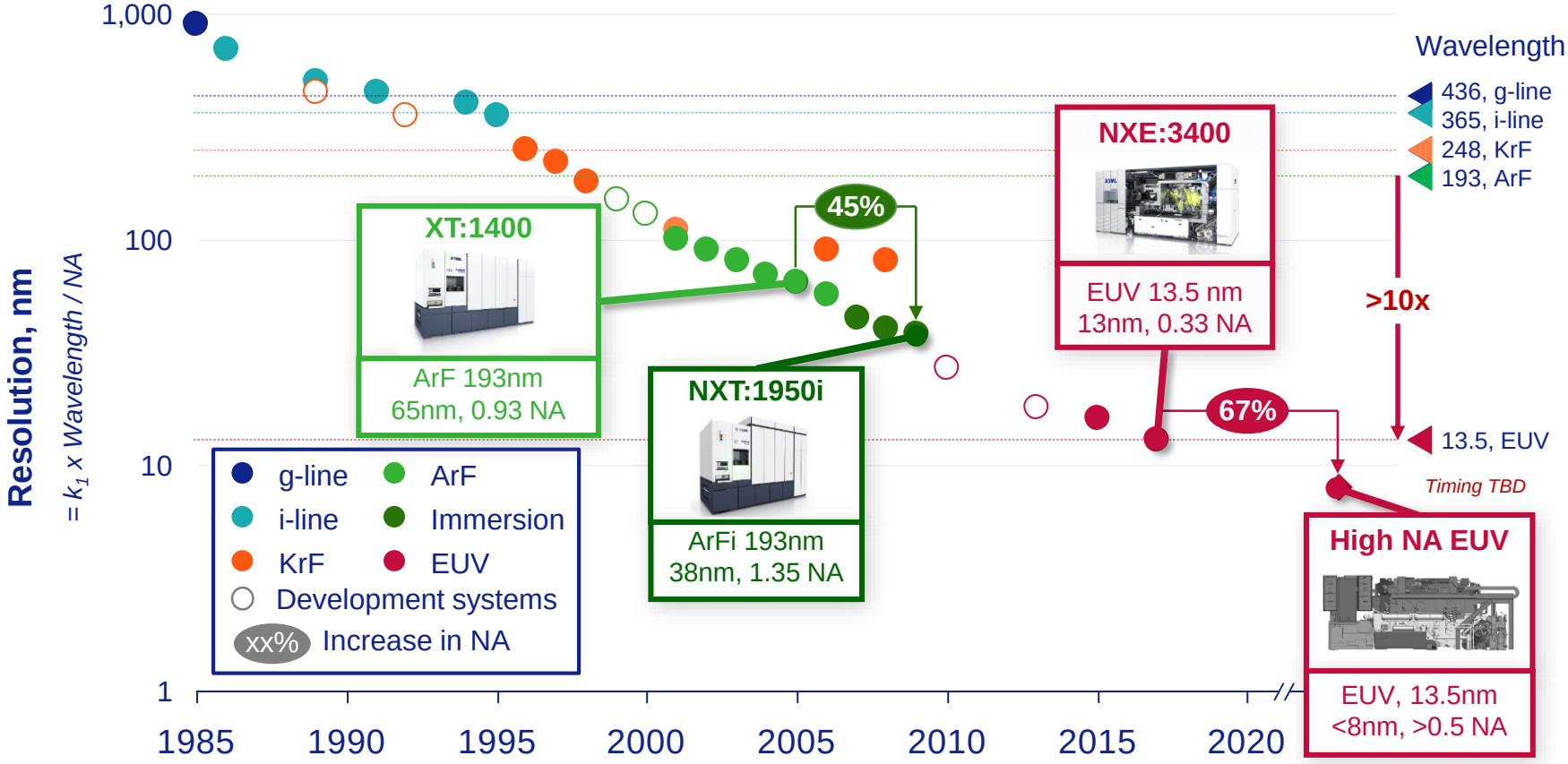
Gary Patton @ Fab 8 Press Tour (Feb 2018)
"(We) will initially offer a 7nm shrink with EUV, that will be used mostly for contacts and vias. This alone may provide a 10 to 15 percent increase in density without a big design investment. When the issues are resolved, EUV can and will be used in many more layers."

What’s next?

Customer roadmaps extend 10 years

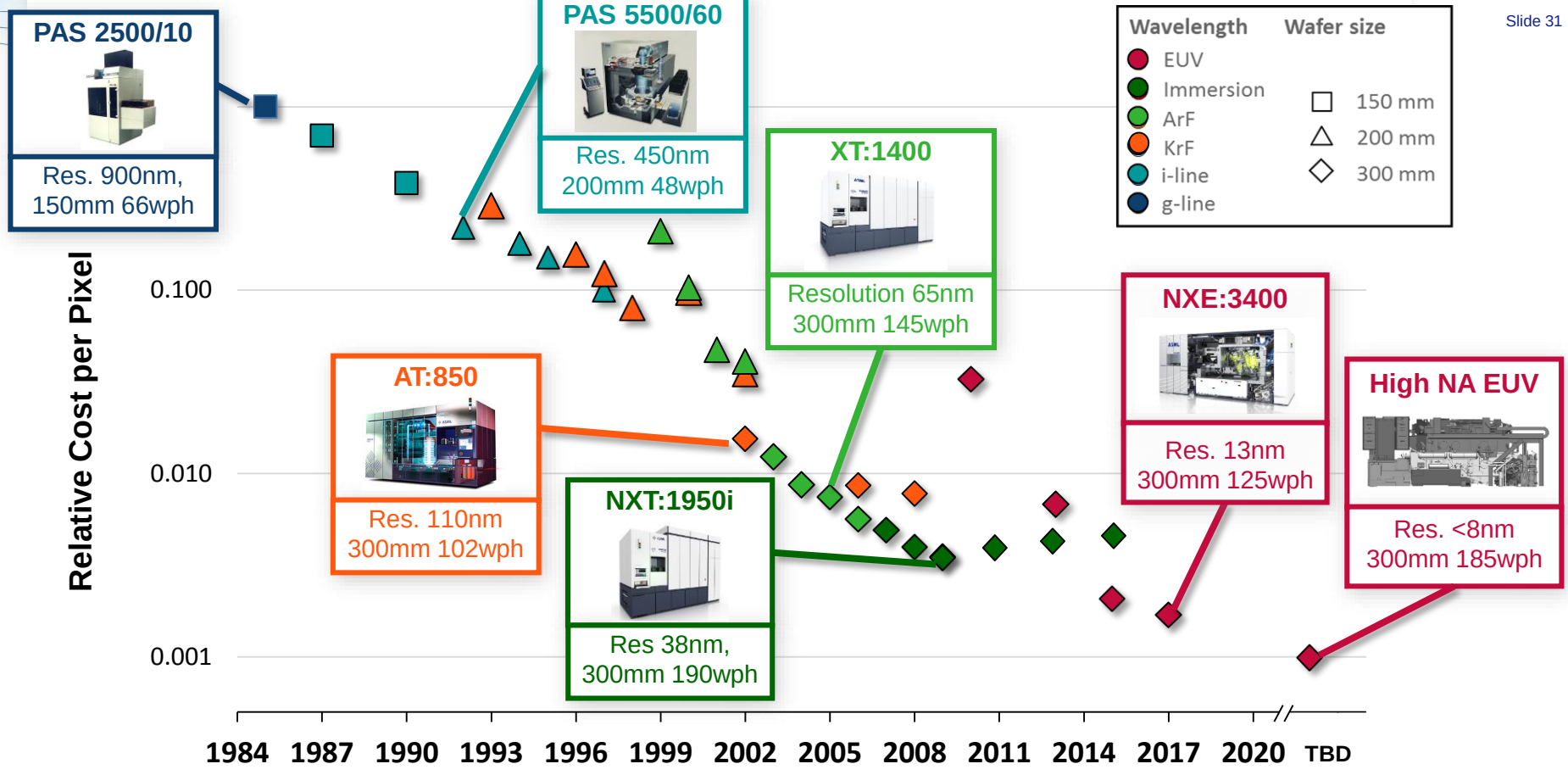


High NA extends EUV with a larger resolution step than immersion did for ArF



High NA EUV extends cost per pixel reduction

ASML

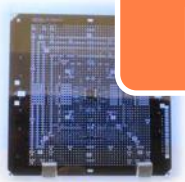


EUV shrink + Holistic Litho (addressing k_1) keeps Moore's Law affordable

Exposure with high order optimisation

Make the image printable and optimize for yield

Keep production stable

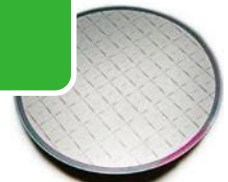


Product reticles

Computational Lithography

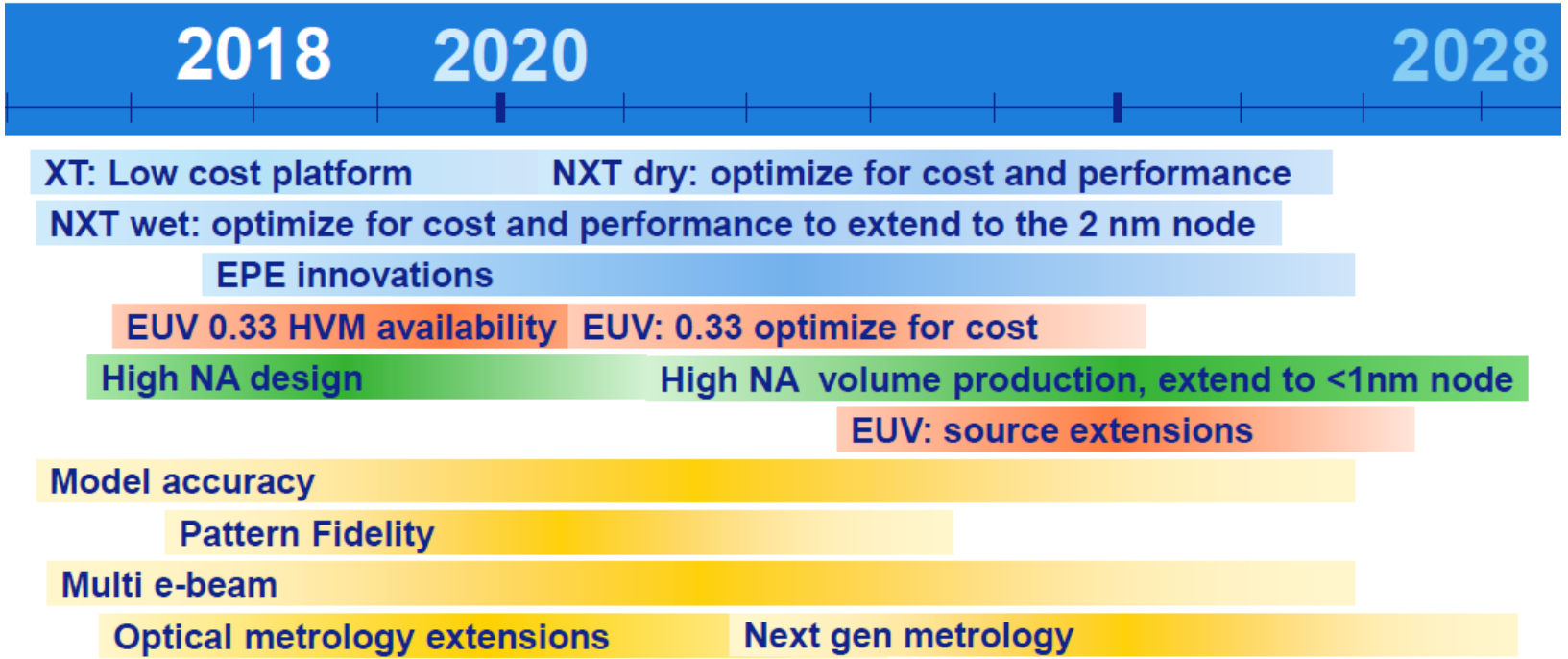
Ensure measurement captures a maximum of relevant information

Optical & e-beam Metrology

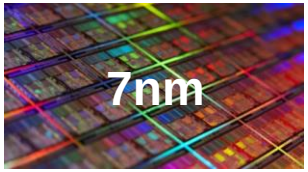


Product wafers

Our innovation pipeline will enable advanced imaging and imaging process control the next 10 years and beyond



EUV Summary



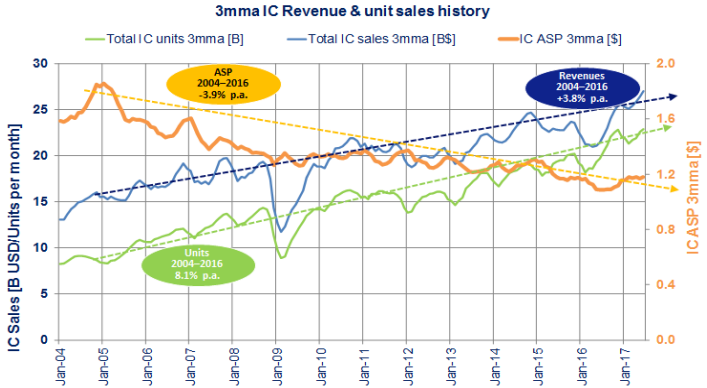
- Customers are targeting EUV introduction at 7nm to take advantage of process complexity, cycle time, IC shrink, yield, & performance benefits

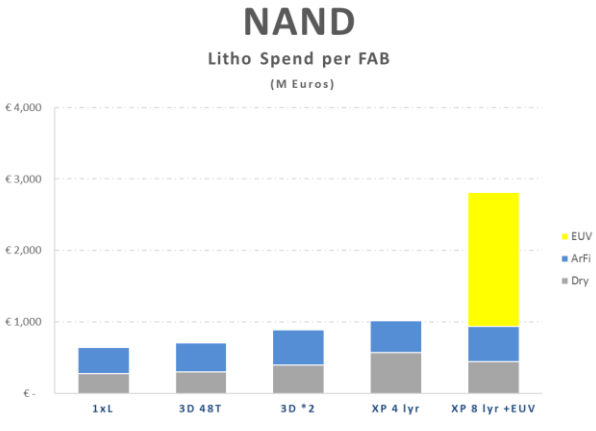
- Key EUV industrialisation & performance milestones have been achieved in 2017, together with solid progress in EUV mask and resist infrastructure

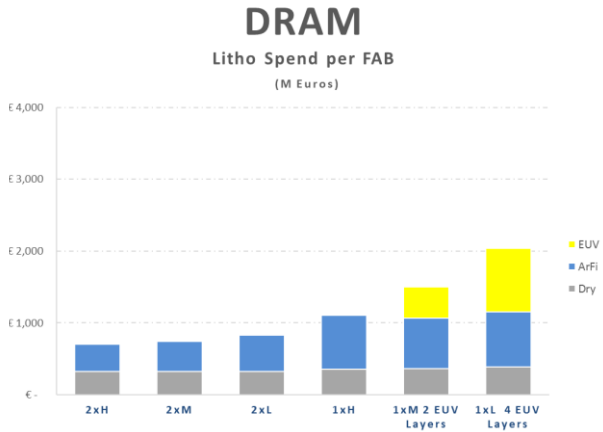
- EUV introduction enables a return to Litho enabled cost reduction with the opportunity to extend multiple generations

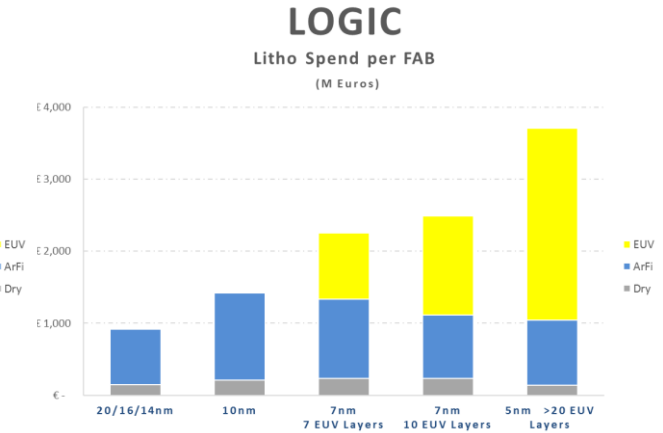
- ASML is investing in a roadmap to enable continued Holistic Lithography scaling for the coming decade

What this means for ASML – As IC units grow and Litho Intensity grows…….. ASML grows!









Summary - Our customers and their environment

- Strong incentives for the entire industry to continue IC performance and cost improvements, now also driving system innovations
- Our logic customers have roadmaps that extend to 2027 and are not planning to slow down scaling
- Memory market is growing and performance improvements continue, enabled by 3D stacking and new scalable memory types. The latter will have an increasing impact the coming 10 years and continue to drive lithography

ASML