128D14 DESIGN NOTES

TABLE OF CONTENTS

Standard Index

A-PART DESCRIPTION / KEY FACTS

B-ARCHITECTURE

C-PROCESS

D-BONDING and/or METAL OPTIONS / DIAGRAMS

E-DATA SHEET (TARGETS AND KEY SPICE RESULTS)

F-TEST MODES / MODE REGISTER

G-ADDRESS / DATA SCRAMBLE

H-FUSE DESCRIPTIONS

I-POWER SUPPLIES

J-SPICE / EPIC METHODS

K-MODELS

L-FILTER CAPS (DESCRIPTION AND VALUES)

M-ESD / LATCHUP

N-CURRENT DENSITY

O-PARASITICS / OFF CURRENT / misc. PROCESS ISSUES

P-LAYOUT (GUIDELINES, LVS/DRC/ERC Rules)

Q-MASK / ALIGNMENT ETC (Not included for this chip).

R-MISCELLANEOUS DESIGN INFORMATION (netlists etc.)

S- RELATED DATA SHEETS (Not included for this chip).

T- GENERAL INFORMATION (NOTES, MEMOS, ETC.) (Currently empty)

A- PART DESCRIPTION / KEY FACTS

128M DDR/SDR/LPSDR S14 Process

4 BANKS
X4 / X8 / X16 BOND OPTION
CLK,DQS,DQ,DM, PINS=SSTL
ADD/CONTROL PINS= SSTL

DDR:
VDD=3.3V or 2.5V
VDDQ=2.5V
UTILIZES DLL
CL 1.5, 2, 2.5, 3
BL 2,4,8
4k REFRESH
Target speed : CL2 =143Mhz
CL3>200Mhz

SDR:
VDD=3.3V or 2.5V
VDDQ=3.3V or 2.5V
CL1,2,3
BL 1,2,4,8,full page
4k REFRESH
Target speed : CL1=83Mhz
CL2=133Mhz
CL3>200Mhz

LPSDR: Same as SDR with special functions for partial array and temperature compensated self refresh.
VDDQ=1.8V

LOC Package
Size = 33.65mm2 (5768x,5833y)
Cell = .1568u2 ~60.45 Efficiency

Reduced Pad test mode. (REDPAD)

**
Design is based on the 128DDR S17 design.

B – ACHITECTURE

The attached diagrams help explain the architecture.

a) 25x plot of the chip
b) diagram of top level LVS cells
c) diagram on 32M bank
d) detailed map of D-F line connections in 32M bank
e) 4M array map
f) map of Sense-Amp band structure between 2 wordline straps (WLS's)
g) stick diagram wordline-bitline-cell placements (for data scramble)
h) diagram of chip's datapath and I/O placements within the arrays.

Other Information:

4 Banks, each bank is a 32Meg array.
Each 32Meg bank has 8 4Meg sub-arrays
512 Cells per Bitline within the 4M sub-arrays
2 Wordlines active in each bank for a cycle (2 sub-arrays are active).

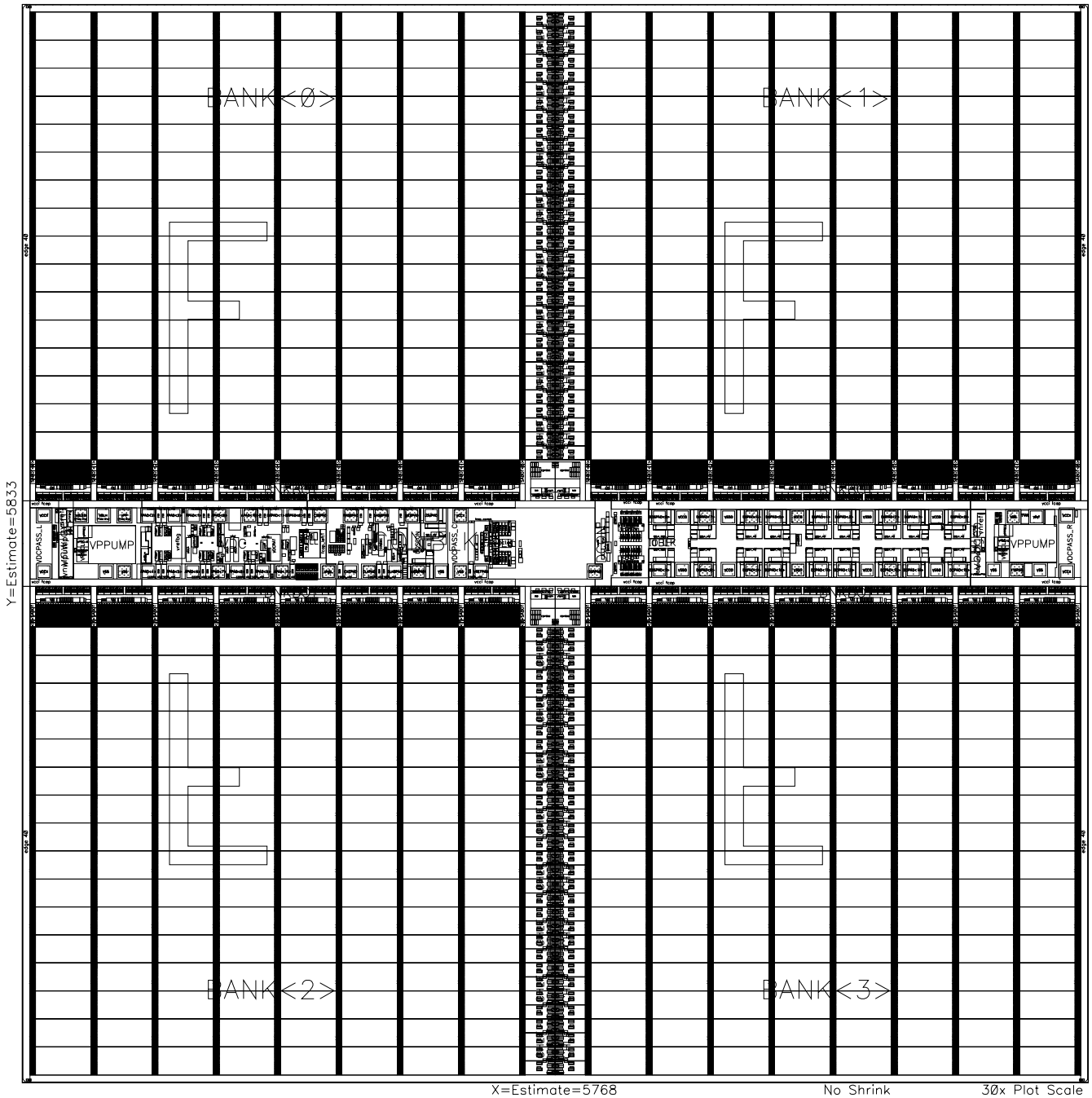
4 Y-selects active per bank for a given read/write cycle.

Global G-Data lines (Read/Write) shared between banks (single ended).
G-bus is 32 bits wide, 16 for rising data, 16 for falling data. (each I/O has rising and falling data associated with it.)

Data Path uses dynamic amplifier (DAMP), it is fully clocked (no wave pipeline).
Control and column circuits work on the system clock.
The read data path works on the DLL clock, key arbitration points are selected for the interfaces.

Write Cycles have latency=1 for DDR
0 for SDR/LPSDR
Refresh = 4K (4 Banks / cycle)
LOC packaging is used

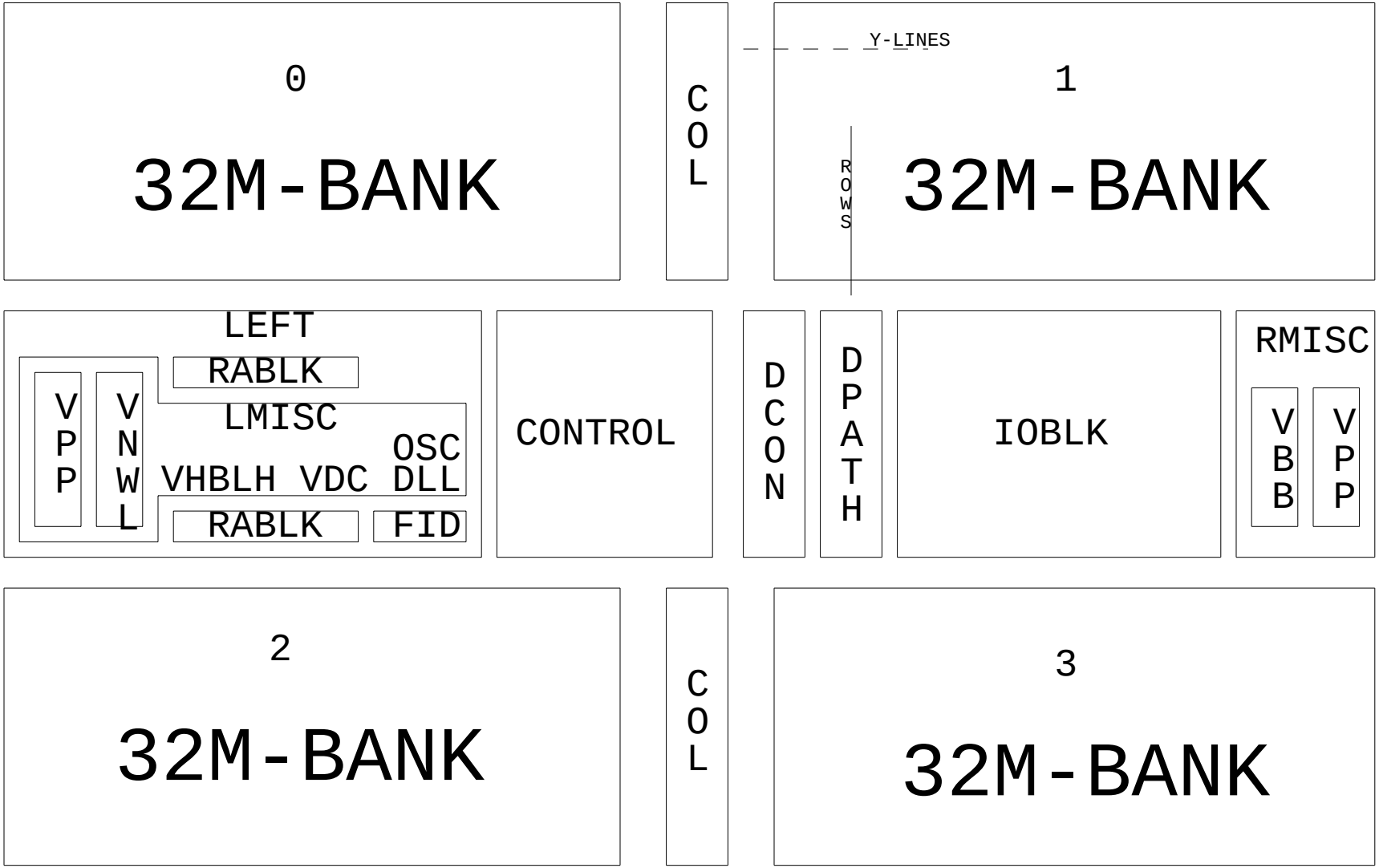
The chip has 9 major sub blocks:
BANK(4x)- the 32Meg arrays
COL(2x)- between two banks, contains all the column decoders, plus data to array amps/drivers.
CONBLK- contains all the control circuitry
DCON- contains the data control circuitry
IOBLK- contains I/O drivers and pads
DPATH- contains data muxes plus shifters for DDR data path implementation
RABLK-contains all address pads, plus Row Address logic and CBR counters
LMISC- Left Side Miscellaneous, VDC, VPL, PUGEN, OSC, DLL, VPP generators.
RMISC- Right Side Miscellaneous including VBB, VPP and test mode circuits.



X=Estimate=5768 No Shrink 30x Plot Scale

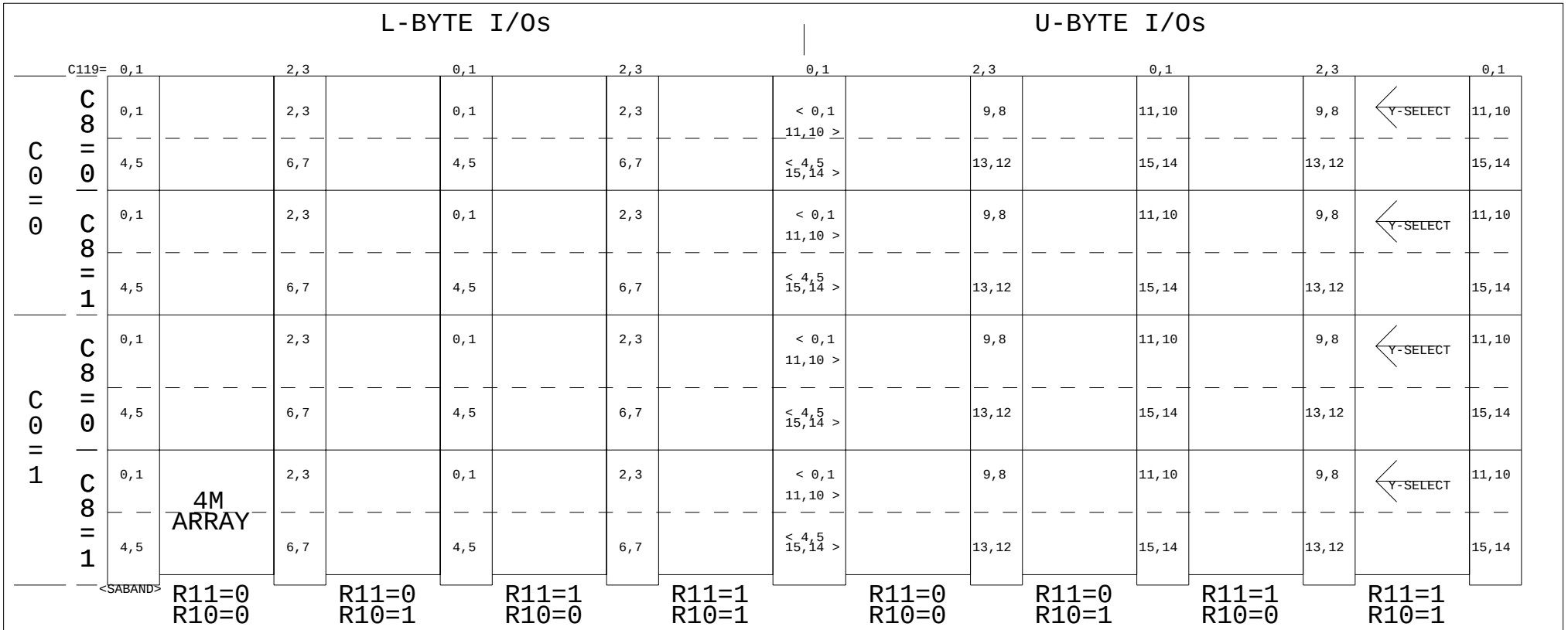
December 21, 2001

128ddr S17 * 0.85x shrink=6943x6953(Chip area=48274679) Cell Efficiency=64.28% (with streets)
256ms14 S14 * 1.0x shrink=11226x5910(Chip area=66345660) Cell Efficiency=63.44% (with streets)
128d14 S14 * 1.0x shrink=5868x5933(Chip area=34814844) Cell Efficiency=60.45% (with streets)
(1024*1024*128=total meg of memory)*memcell area(.1568)/chip area including 100um streets for X and Y



NOT TO SCALE

UNITED MEMORIES, INC. PROJECT: 128D14		
Title LVS Architecture		
Size A	Document Number LVSARCH	REV A
Date: December 21, 2001	Sheet 1 of 1	



CORRECT FOR BANKS 0,1

(C0 IS OPPOSITE FOR BANKS 2,3)
(U & L BYTES ARE OPPOSITE FOR BANKS 2,3)

2 4M ARRAYS ACTIVE FOR EACH ROW CYCLE.
1 WORDLINE IN EACH 4M ARRAY.
SABAND TO LEFT AND RIGHT OF ACTIVE WORDLINE OUTPUTS DATA.
(8 BITS TOTAL/SABAND)
(32 BITS TOTAL PER BANK, 16 EVEN, 16 ODD)

CENTER CASE SABAND IS EITHER L-BYTE OR U-BYTE,
DEPENDING UPON THE ROW ADDRES SELECTED.

4 Y-SELECTS ACTIVE PER BANK, FOR EACH READ/WRITE CYCLE.
EACH Y-SELECT GETS 8 BITS.

	C119 <0>	<1>	<2>	<3>
L-BYTE	IO <0>	<1>	<2>	<3>
	IO <4>	<5>	<6>	<7>
U-BYTE	IO<11>	<10>	<9>	<8>
	IO<15>	<14>	<13>	<12>
	X8		X8 X4	

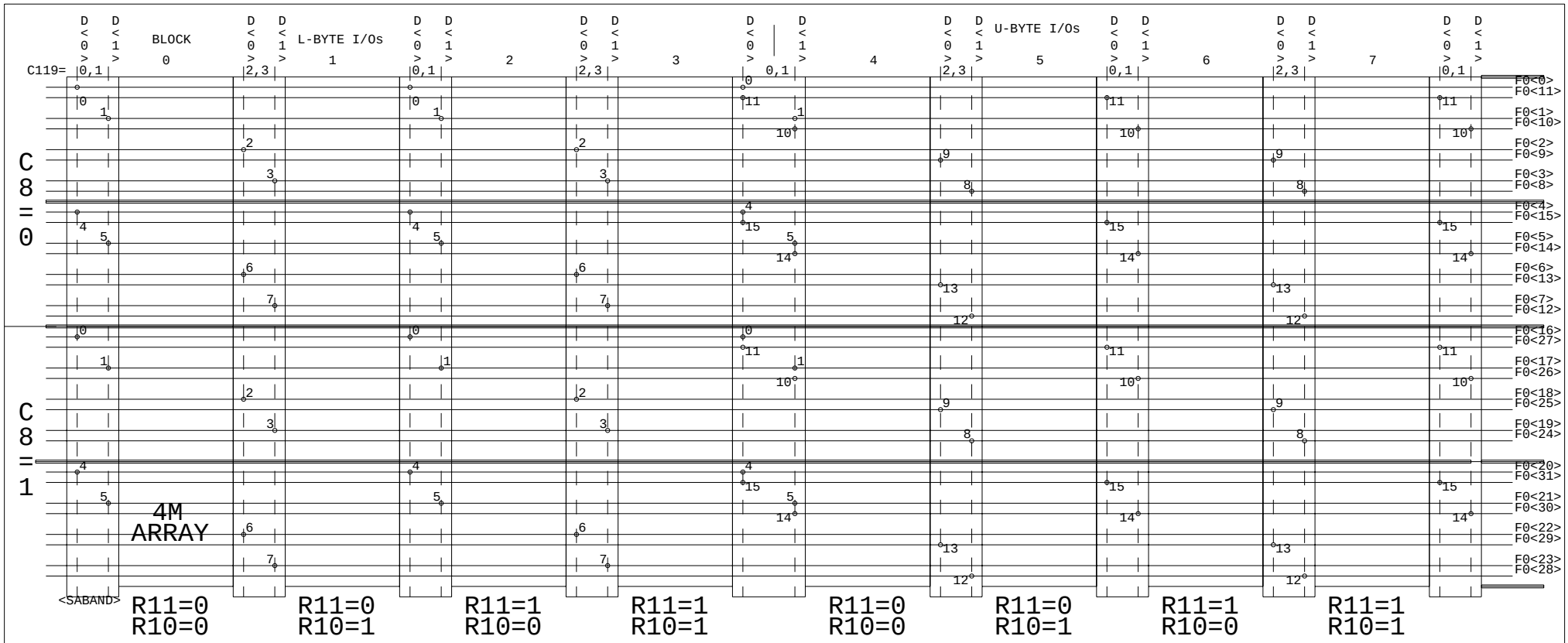
FOR X16 / ALL ON

United Memories Inc
PROJECT: 128D14

Title: 32M ARY MAP (1 BANK)P

Size: B | Document Number: MAP32M | REV: A

Date: December 21, 2001 | Sheet of



(1/2 OF BANKS 0,1)

THIS CASE REPRESENTS THE C0=0 CASE.
FOR C0=1 CASE, F0<X> MAPS TO F1<X>.

Top half of bank.
Lower half is a step
of upper half with
F0<x> replaced with F1<x>.

CORRECT FOR BANKS 0,1

2 4M ARRAYS ACTIVE FOR EACH ROW CYCLE.
1 WORDLINE IN EACH 4M ARRAY.
SABAND TO LEFT AND RIGHT OF ACTIVE WORDLINE OUTPUTS DATA.
(8 BITS TOTAL/SABAND)
(32 F-LINES TOTAL PER BANK, 32 EVEN, 32 ODD)

CENTER CASE SABAND IS EITHER L-BYTE OR U-BYTE,
DEPENDING UPON THE ROW ADDRES SELECTED.

4 Y-SELECTS ACTIVE PER BANK, FOR EACH READ/WRITE CYCLE.
EACH Y-SELECT GETS 8 BITS.

	C119 <0>	<1>	<2>	<3>
L-BYTE	IO <0>	<1>	<2>	<3>
	IO <4>	<5>	<6>	<7>
U-BYTE	IO<11>	<10>	<9>	<8>
	IO<15>	<14>	<13>	<12>
	X8		X8 X4	

FOR X16 / ALL ON

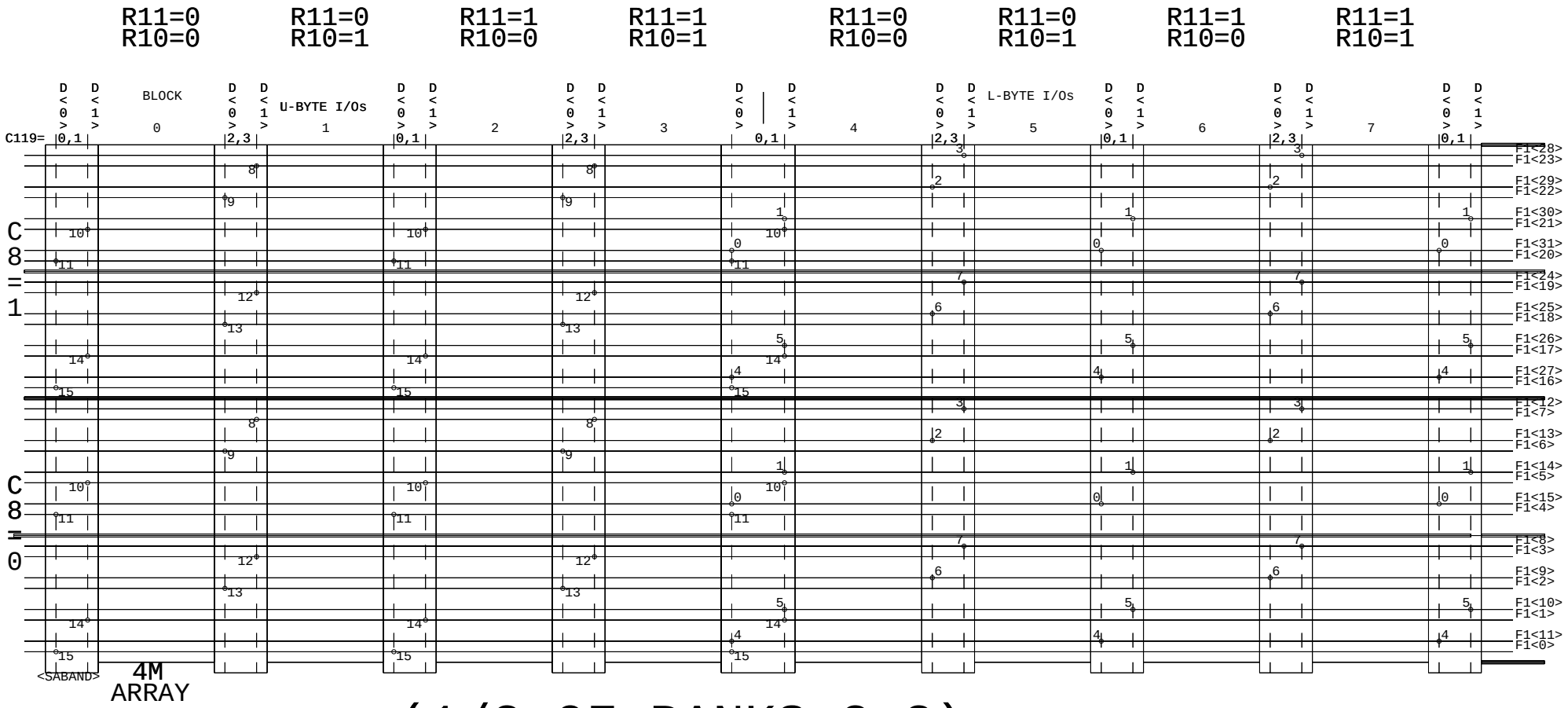
VALID FOR 1 BANK

United Memories Inc
PROJECT: 128D14

Title
F-LINES TO D-LINES (VIA SHMUX) MAP

Size	Document Number	REV
B	MAPFD	A

Date: December 21, 2001 Sheet of



(1/2 OF BANKS 2,3)

Top half of bank.
Lower half is a step
of upper half with
F1<x> replaced with F0<x>.

THIS CASE REPRESENTS THE C0=0 CASE.
FOR C0=1 CASE, F1<X> MAPS TO F0<X>.

	C119 <0>	<1>	<2>	<3>
L-BYTE	IO <0>	<1>	<2>	<3>
	IO <4>	<5>	<6>	<7>
U-BYTE	IO<11>	<10>	<9>	<8>
	IO<15>	<14>	<13>	<12>
	X8		X8 X4	

FOR X16 / ALL ON

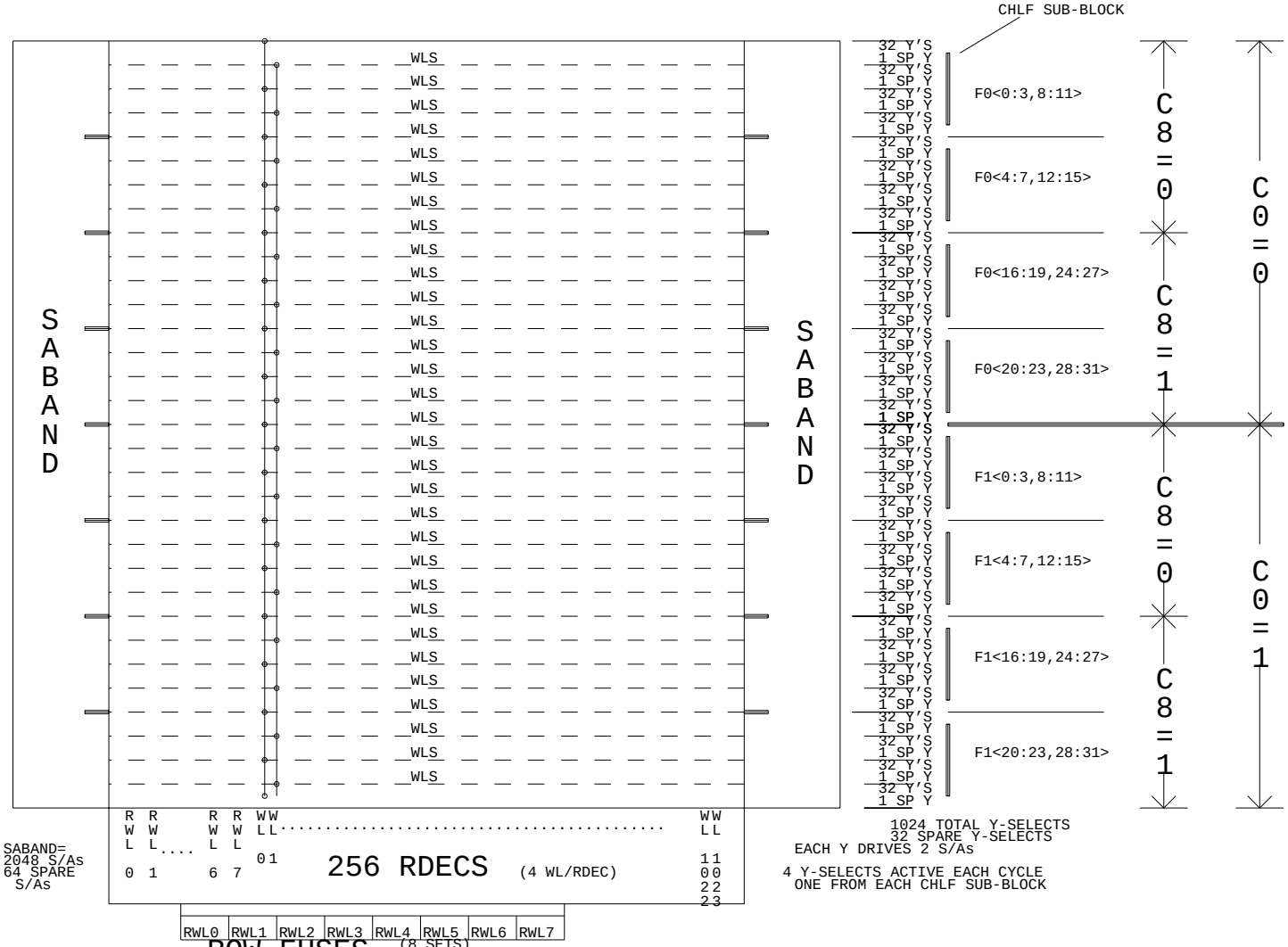
VALID FOR 1 BANK

United Memories Inc
PROJECT: 128D14

Title
F-LINES TO D-LINES (VIA SHMUX) MAP

Size	Document Number	REV
B	MAPFF	A

Date: December 21, 2001 Sheet of



SABAND=
2048 S/As
64 SPARE
S/As

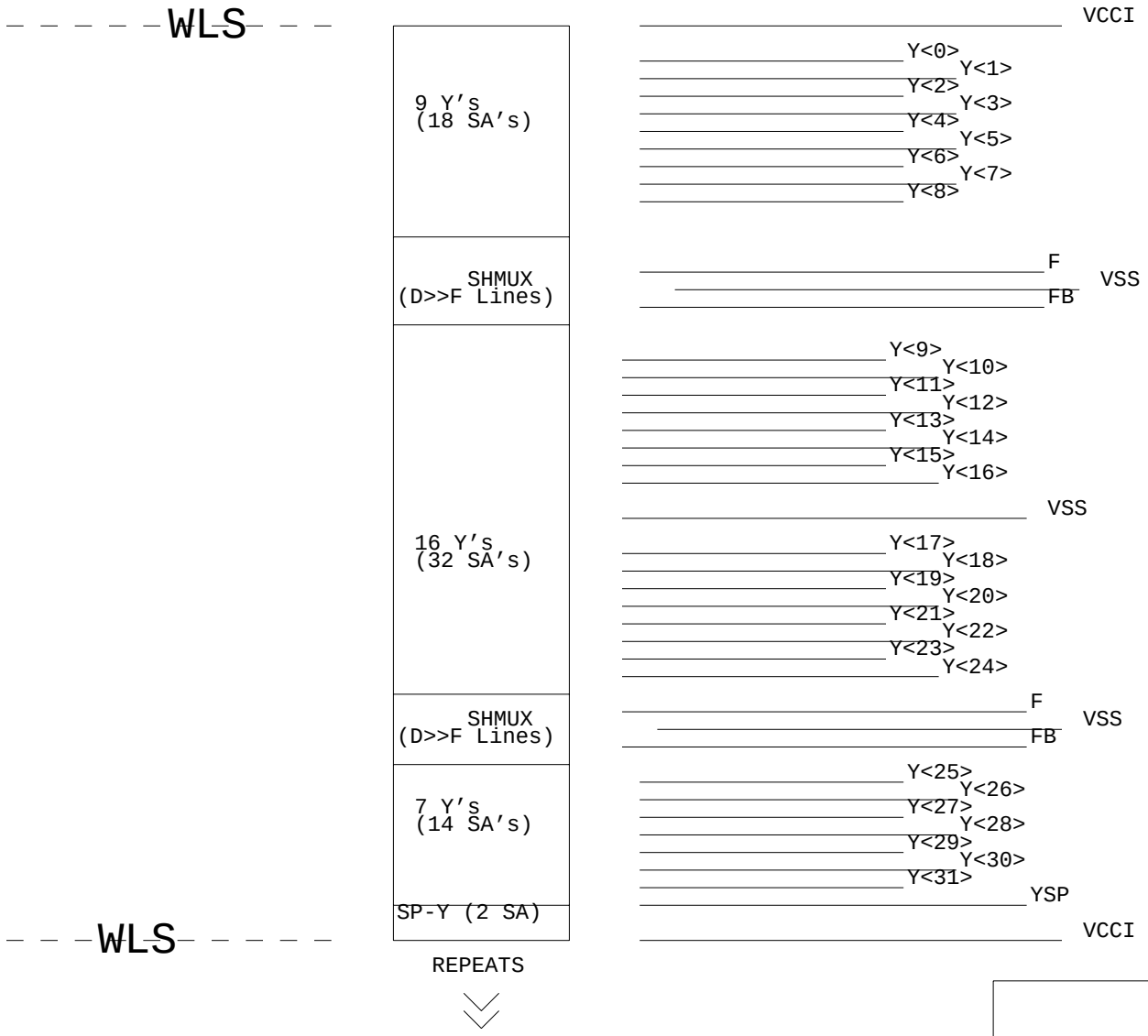
1024 TOTAL Y-SELECTS
32 SPARE Y-SELECTS
EACH Y DRIVES 2 S/As

4 Y-SELECTS ACTIVE EACH CYCLE
ONE FROM EACH CHLF SUB-BLOCK

WLS=WORDLINE STRAP
NOTE-EACH WORDLINE IS TIED AT
EVERY OTHER WLS LOCATION

NOT TO SCALE

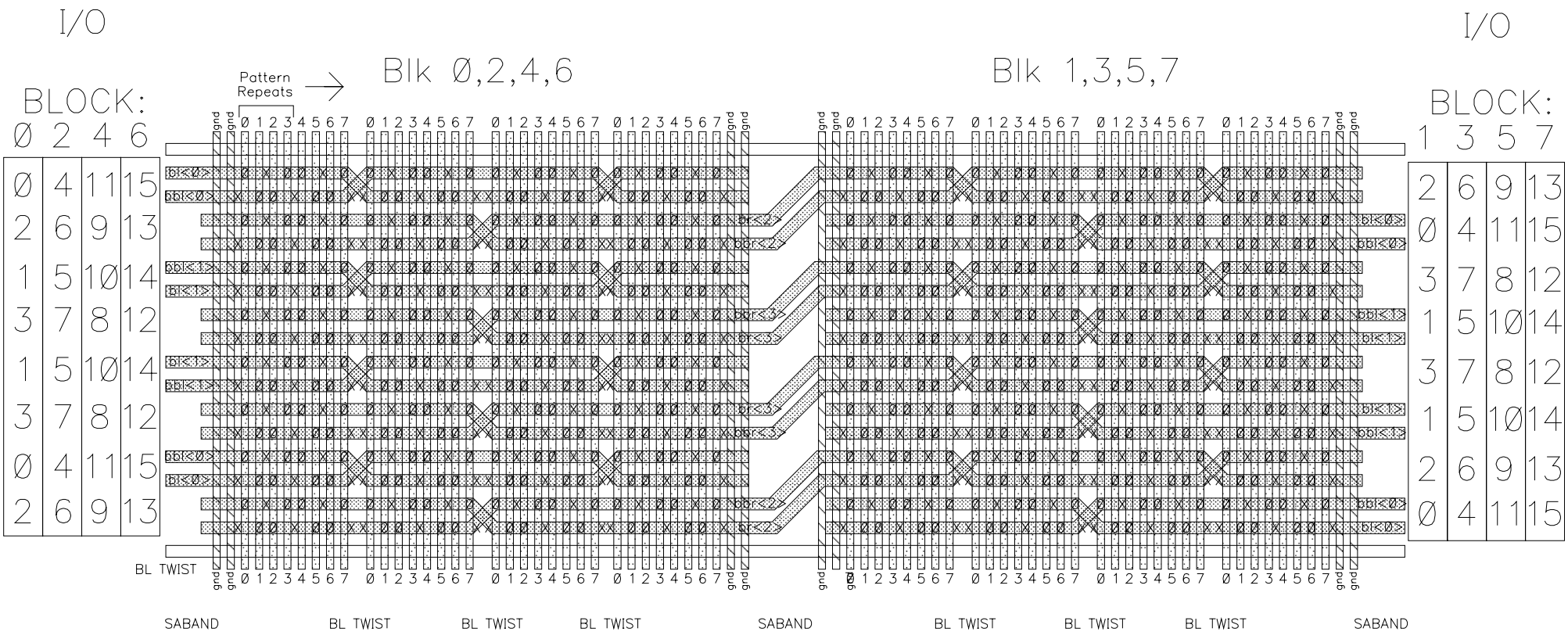
UNITED MEMORIES, INC. PROJECT: 128D14		
Title MAP OF 4M ARRAY		
Size B	Document Number MAP4M	REV A
Date: December 21, 2001	Sheet 1 of 1	



NOT TO SCALE

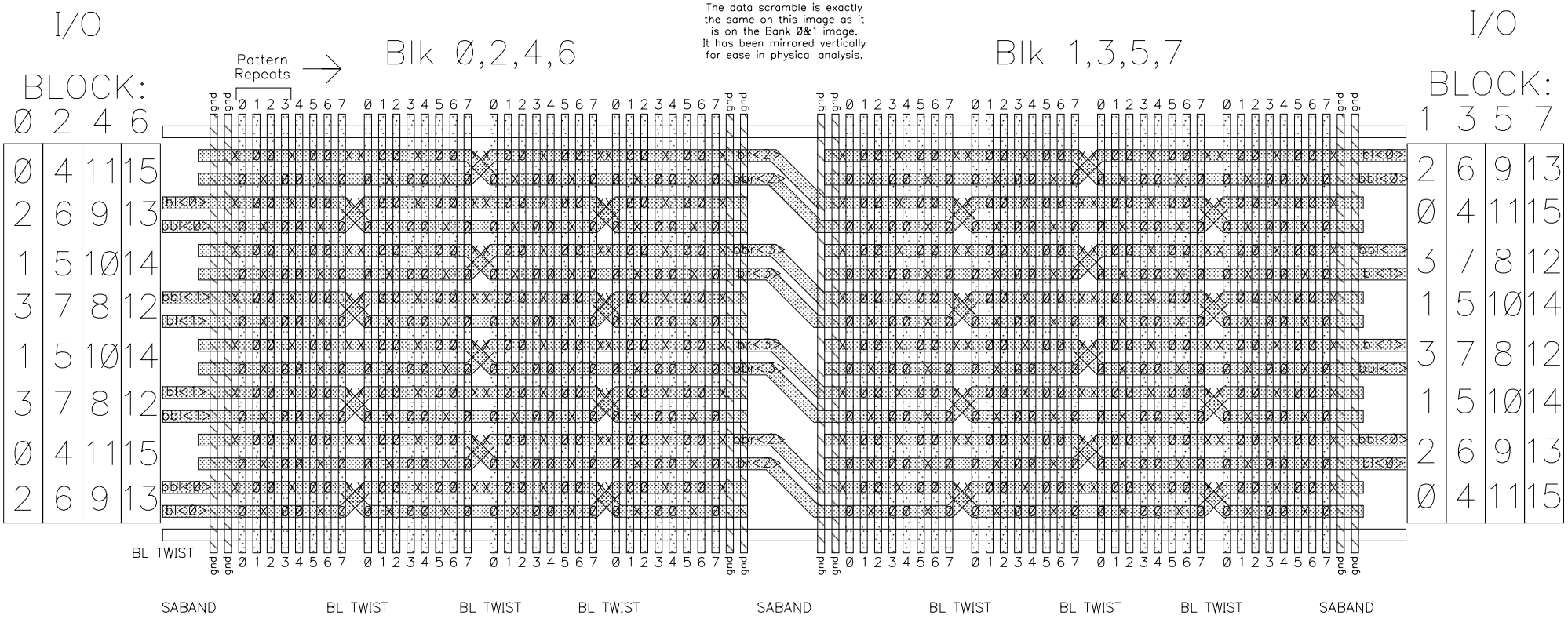
UNITED MEMORIES, INC. PROJECT: 128D14		
Title MAP OF AREA BETWEEN WLS's		
Size A	Document Number MAPWLS	REV A
Date: December 21, 2001	Sheet 1 of 1	

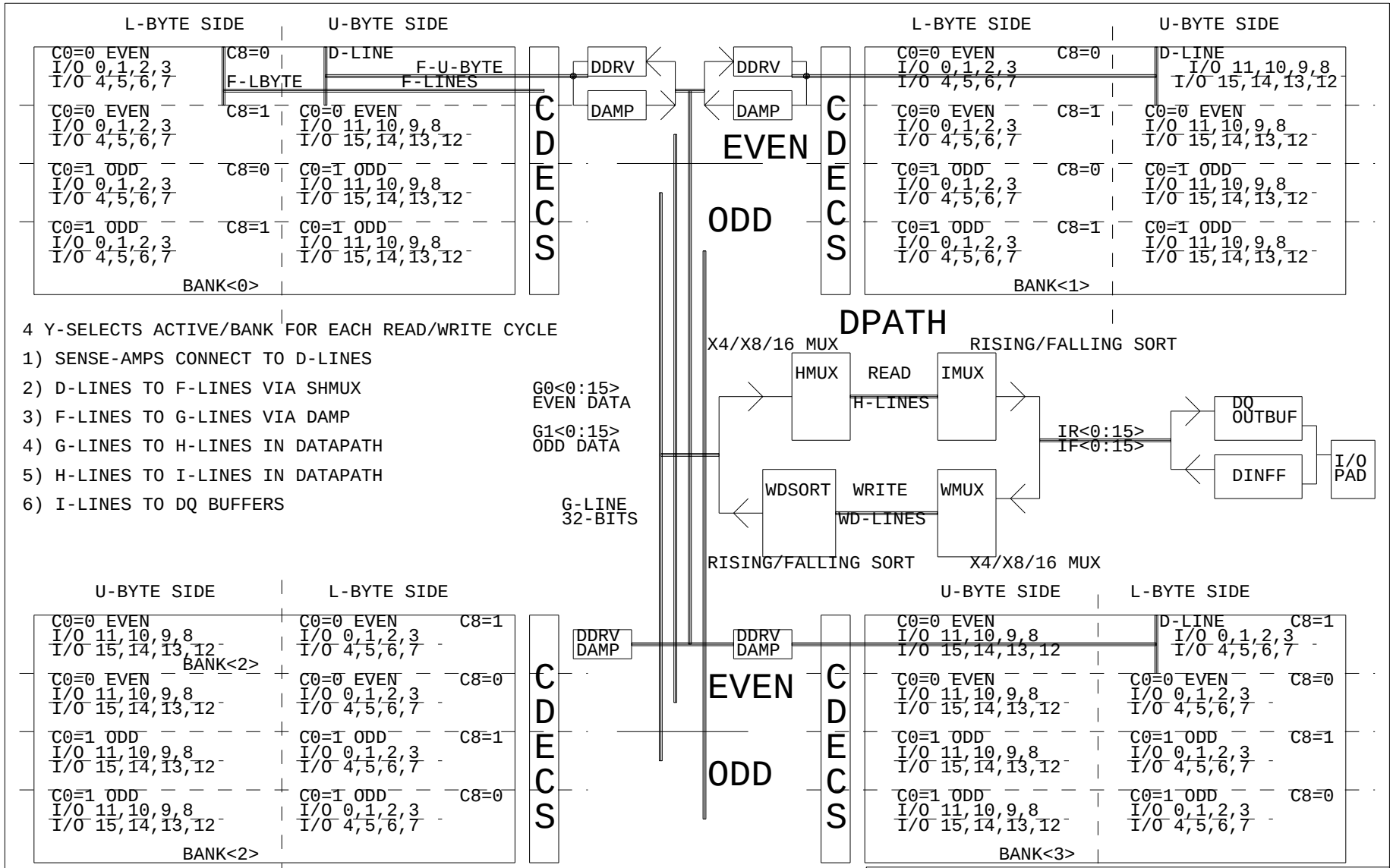
Bank Ø & 1


I/O
BLOCK:
Ø 2 4 6
Pattern Repeats
Blk Ø,2,4,6
Blk 1,3,5,7
I/O
BLOCK:
1 3 5 7
BL TWIST
SABAND
BL TWIST
BL TWIST
BL TWIST
SABAND
BL TWIST
BL TWIST
BL TWIST
SABAND

Bank 2 & 3

The data scramble is exactly the same on this image as it is on the Bank Ø&1 image. It has been mirrored vertically for ease in physical analysis.





4 Y-SELECTS ACTIVE/BANK FOR EACH READ/WRITE CYCLE

1) SENSE-AMPS CONNECT TO D-LINES
2) D-LINES TO F-LINES VIA SHMUX
3) F-LINES TO G-LINES VIA DAMP
4) G-LINES TO H-LINES IN DATAPATH
5) H-LINES TO I-LINES IN DATAPATH
6) I-LINES TO DQ BUFFERS

DATA COMPRESSION TABLE

C119=	0	1	2	3
F/DQ=	0	1	2	3
F/DQ=	4	5	6	7
F/DQ=	11	10	9	8
F/DQ=	15	14	13	12

X8-EVEN DQ's ACTIVE
X4-2,6,9,13 DQ's ACTIVE

2 WORDLINES ACTIVE IN EACH BANK
-ONE IN L-BYTE HALF
-ONE IN U-BYTE HALF

EVEN TO ODD DATA PATH "STEPS" DOWN, NOT MIRRORED. A BIT ALWAYS STAYS IN THE SAME C119(X) COLUMN SO THE SCRAMBLE IS THE SAME IN ANY BANK!!

UNITED MEMORIES, INC.
PROJECT: 128D14

Title: DATA PATH Architecture

Size	Document Number	REV
A	DPARCH	A

Date: December 21, 2001 | Sheet 1 of 1

upper banks (0,1)

```
 F          connects          which connects
Line        to upper          upper G line
            G line            (I/O)

C8=0, C0=0
F0<0>       G0<0>             G0<0>                   Y=0
F0<11>      G0<11>            G0<11>
F0<1>       G0<1>             G0<1>
F0<10>      G0<10>            G0<10>
F0<2>       G0<2>             G0<2>
F0<9>       G0<9>             G0<9>
F0<3>       G0<3>             G0<3>
F0<8>       G0<8>             G0<8>

F0<4>       G0<4>             G0<4>
F0<15>      G0<15>            G0<15>
F0<5>       G0<5>             G0<5>
F0<14>      G0<14>            G0<14>
F0<6>       G0<6>             G0<6>
F0<13>      G0<13>            G0<13>
F0<7>       G0<7>             G0<7>
F0<12>      G0<12>            G0<12>

C8=1, C0=0
F0<16>      G0<0>
F0<27>      G0<11>
F0<17>      G0<1>
F0<26>      G0<10>
F0<18>      G0<2>
F0<25>      G0<9>
F0<19>      G0<3>
F0<24>      G0<8>

F0<20>      G0<4>
F0<31>      G0<15>
F0<21>      G0<5>
F0<30>      G0<14>
F0<22>      G0<6>
F0<29>      G0<13>
F0<23>      G0<7>
F0<28>      G0<12>
------------------------
C8=0, C0=1
F1<0>       G1<0>             G1<0>       |
F1<11>      G1<11>            G1<11>      |
F1<1>       G1<1>             G1<1>       |           128 y lines
F1<10>      G1<10>            G1<10>      | Dline     4 spare y lines
F1<2>       G1<2>             G1<2>       | length
F1<9>       G1<9>             G1<9>       |
F1<3>       G1<3>             G1<3>       |
F1<8>       G1<8>             G1<8>       |

F1<4>       G1<4>             G1<4>
F1<15>      G1<15>            G1<15>
F1<5>       G1<5>             G1<5>
```

```
F1<14>      G1<14>            G1<14>
F1<6>       G1<6>             G1<6>
F1<13>      G1<13>            G1<13>
F1<7>       G1<7>             G1<7>
F1<12>      G1<12>            G1<12>

C8=1, C0=1
F1<16>      G1<0>
F1<27>      G1<11>
F1<17>      G1<1>
F1<26>      G1<10>
F1<18>      G1<2>
F1<25>      G1<9>
F1<19>      G1<3>
F1<24>      G1<8>

F1<20>      G1<4>
F1<31>      G1<15>
F1<21>      G1<5>
F1<30>      G1<14>
F1<22>      G1<6>
F1<29>      G1<13>
F1<23>      G1<7>
F1<28>      G1<12>                                  Y=1023
```

Lower banks (2,3)

```
 F          connects          which connects
Line        to lower          upper G line
            G line            (I/O)

C8=1, C0=0
F1<28>      G1<12>            G0<3>                   Y=1023
F1<23>      G1<7>             G0<8>
F1<29>      G1<13>            G0<2>
F1<22>      G1<6>             G0<9>
F1<30>      G1<14>            G0<1>
F1<21>      G1<5>             G0<10>
F1<31>      G1<15>            G0<0>
F1<20>      G1<4>             G0<11>

F1<24>      G1<8>             G0<7>
F1<19>      G1<3>             G0<12>
F1<25>      G1<9>             G0<6>
F1<18>      G1<2>             G0<13>
F1<26>      G1<10>            G0<5>
F1<17>      G1<1>             G0<14>
F1<27>      G1<11>            G0<4>
F1<16>      G1<0>             G0<15>

C8=0, C0=0
F1<12>      G1<12>
F1<7>       G1<7>
F1<13>      G1<13>
F1<6>       G1<6>
F1<14>      G1<14>
F1<5>       G1<5>
F1<15>      G1<15>
F1<4>       G1<4>

F1<8>       G1<8>
F1<3>       G1<3>
F1<9>       G1<9>
F1<2>       G1<2>
F1<10>      G1<10>
F1<1>       G1<1>
F1<11>      G1<11>
F1<0>       G1<0>
------------------------
C8=1, C0=1
F0<28>      G0<12>            G1<3>       |
F0<23>      G0<7>             G1<8>       |
F0<29>      G0<13>            G1<2>       |           128 y lines
F0<22>      G0<6>             G1<9>       | Dline     4 spare y lines
F0<30>      G0<14>            G1<1>       | length
F0<21>      G0<5>             G1<10>      |
F0<31>      G0<15>            G1<0>       |
F0<20>      G0<4>             G1<11>      |

F0<24>      G0<8>             G1<7>
F0<19>      G0<3>             G1<12>
F0<25>      G0<9>             G1<6>
```

```
F0<18>      G0<2>             G1<13>
F0<26>      G0<10>            G1<5>
F0<17>      G0<1>             G1<14>
F0<27>      G0<11>            G1<4>
F0<16>      G0<0>             G1<15>

C8=0, C0=1
F0<12>            G0<12>
F0<7>             G0<7>
F0<13>            G0<13>
F0<6>             G0<6>
F0<14>            G0<14>
F0<5>             G0<5>
F0<15>            G0<15>
F0<4>             G0<4>

F0<8>             G0<8>
F0<3>             G0<3>
F0<9>             G0<9>
F0<2>             G0<2>
F0<10>            G0<10>
F0<1>             G0<1>
F0<11>            G0<11>
F0<0>             G0<0>                                Y=0
```

C – PROCESS

Designed for the Pro-MOS S14 Process (Infineon's)

A 0.14um process

triple-well
Shallow trench isolation
Deep trench memory cell
CMP planarization utilized

Wordlines in M1, on pitch strapping, (no local wordline drivers).
M0 bitlines
M1 fuses
M2 is top interconnect layer (Y-lines, data lines)

See "0.14um Design Manual for DRAM Products" for complete list of process features.

The Design Rules are included here, hopefully they are up to date. (Section P).

D – BONDING and/or METAL OPTIONS / DIAGRAMS

The following table defines the bonding options for the various modes.
Note: A "—" indicates that this pad is used in this mode and is not a bond option pad.

Mode	DDR	DQ7	DQ8	X16	DQS<1>
X16 DDR	VCCX	--	--	VCCX	--
X8 DDR	VCCX	VSSQ	VCCQ	VSS	--
X4 DDR	VCCX	VCCQ	VSSQ	VSS	--
X16 SDR	VSS	--	--	VCCX	VCCX
X8 SDR	VSS	VSSQ	VCCQ	VSS	VCCX
X4 SDR	VSS	VCCX	VSS	VSS	VCCX
X16 LPSDR	VSS	--	--	VCCX	VSS
X8 LPSDR	VSS	VSSQ	VCCQ	VSS	VSS
X4 LPSDR	VSS	VCCX	VSS	VSS	VSS
REDPAD	N/C	VSS	VSS	VSS	N/C

Twelve sample bonding diagrams are attached:DDR,SDR,LPSDR,X16,X8,X4.

For x4 and x8 modes, all unused I/O pads are shorted to VSS except
I/Os 7 and 8.
(DO NOT PROBE !)

****

IN / OT (in and out M2 options)

These are in the schematics to show potential M2 changes for timing / function edits.

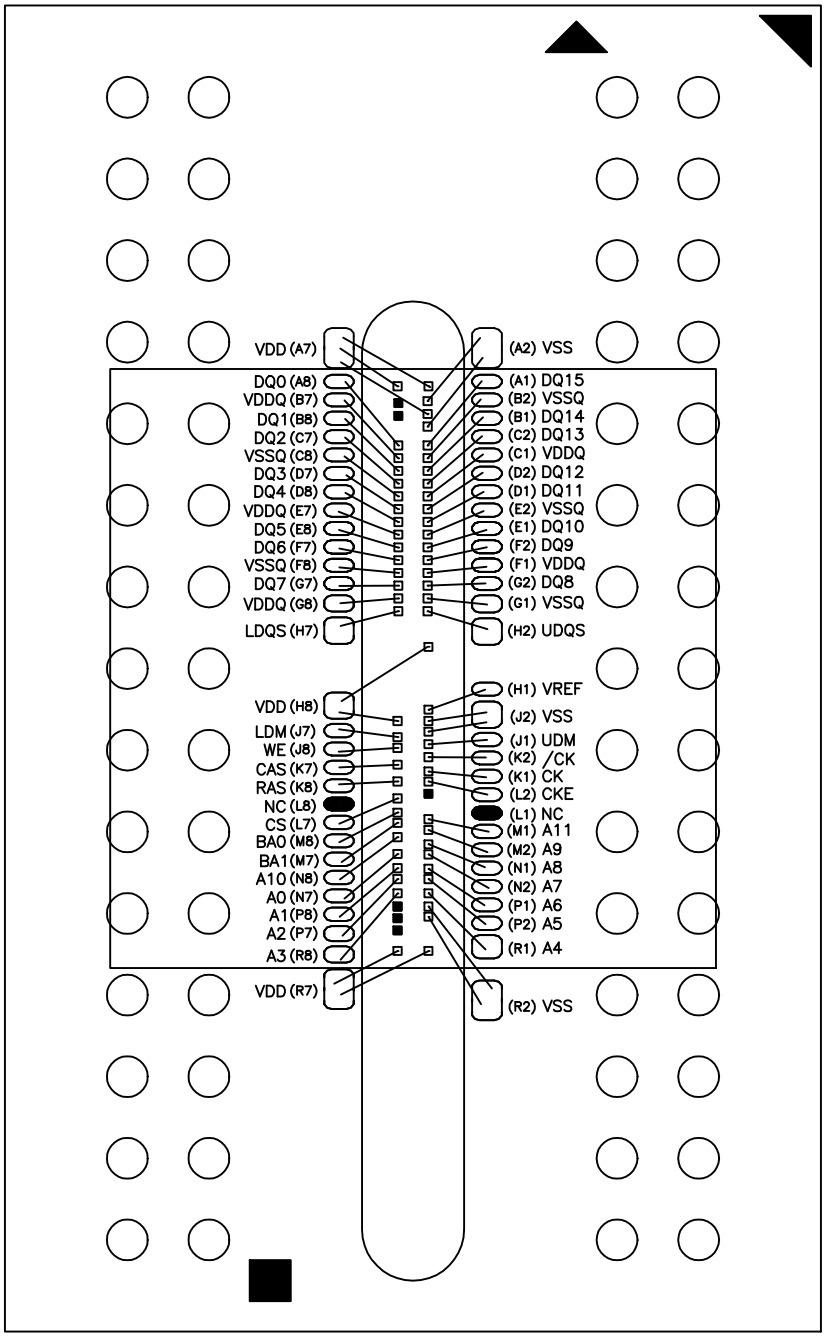
The IN layer is already merged with M2, so nothing needs to be done during fracture.
These are very useful with the FIB machine.

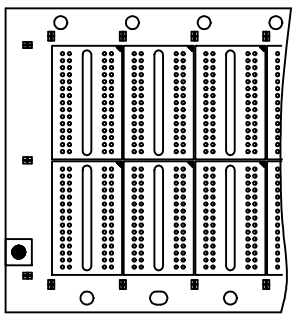
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

從VSS開始銲線
Start from VSS

Approved By

DDR SDRAM (x16)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C2,C1,E7,E2,K7,K8,K1,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 65
REMARKS	: Max wire length is 1.06mm(42mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 120um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14u)
8Mx16 (128MB) DDR SDRAM (0.17um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/19/2001	12/19/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1018A

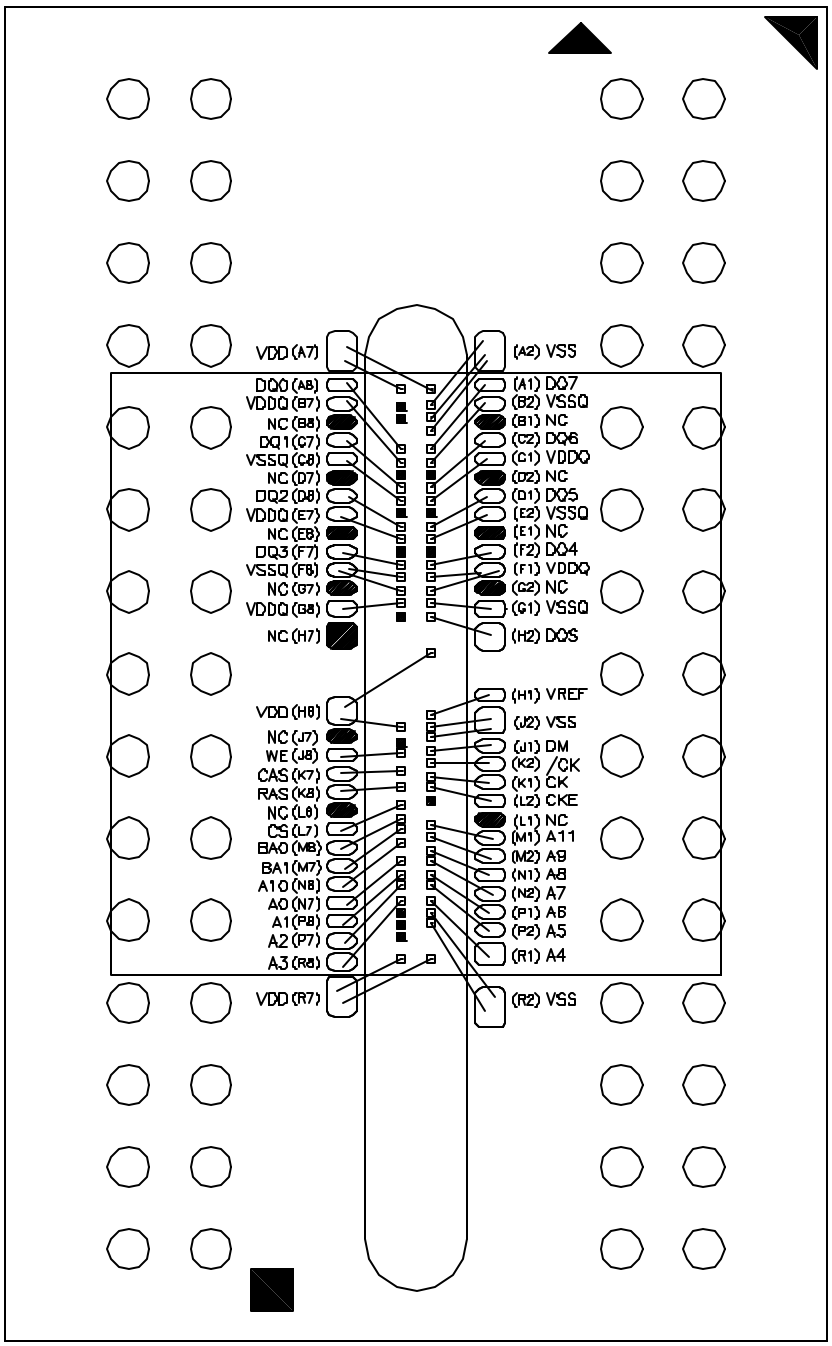
SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

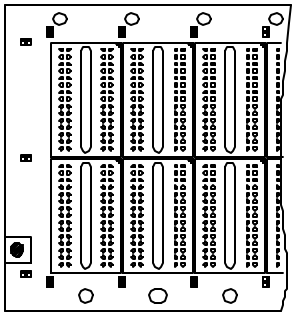
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

從VSS開始銲線
Start from VSS

Approved By

DDR SDRAM (x8)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C2,C1,E7,E2,K7,K8,K1,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 57
REMARKS	: Max wire length is 1.06mm(42mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 120um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14u)
16Mx8 (128MB) DDR SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/24/2001	12/24/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1017A

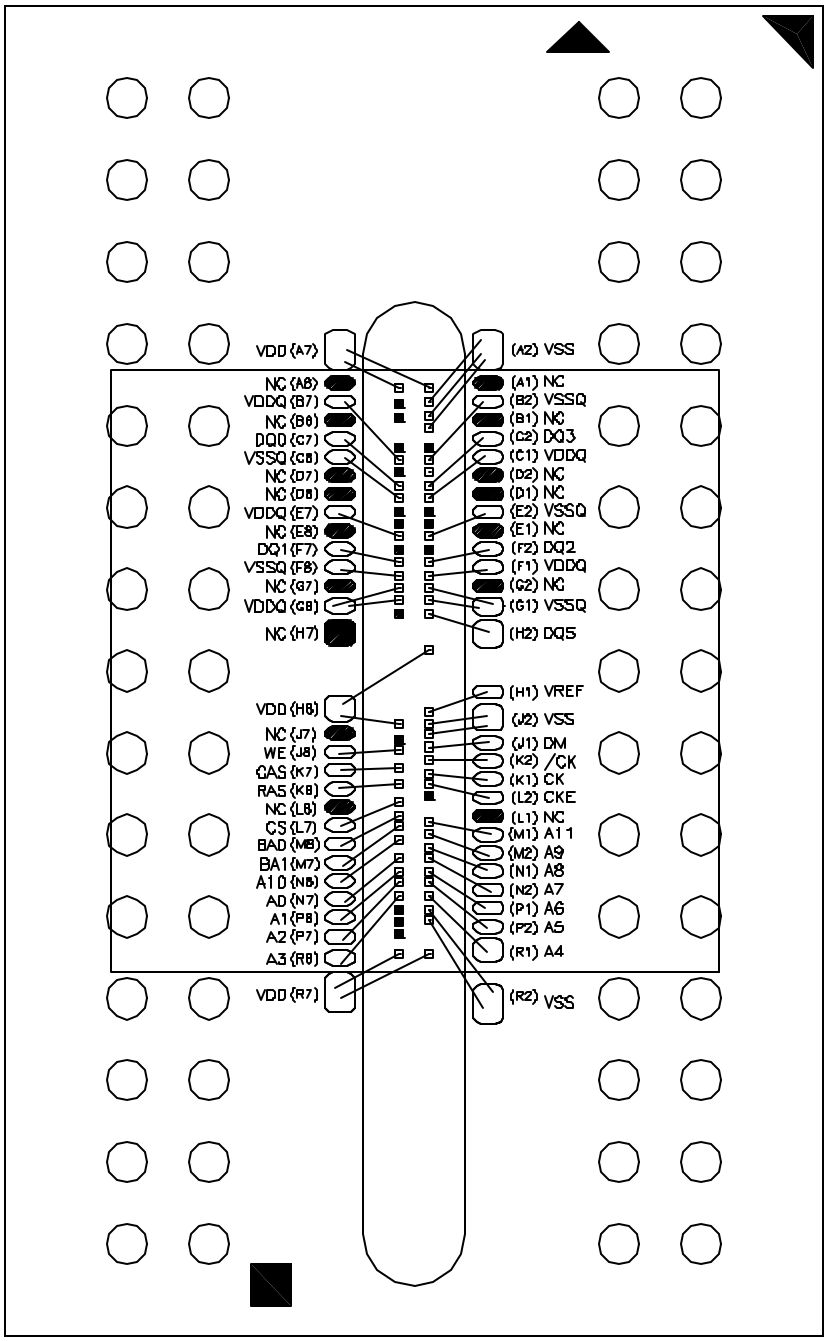
SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

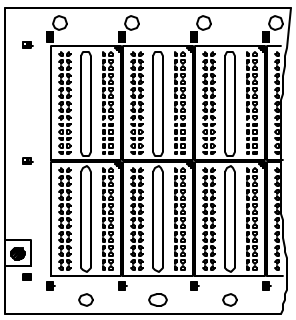
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

從VSS開始銲線
Start from VSS

Approved By

DDR SDRAM (x4)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C2,C1,E7,E2,K7,K8,K1,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 53
REMARKS	: Max wire length is 1.06mm(42mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 120um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14u)
32Mx4 (128MB) DDR SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/24/2001	12/24/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1016A

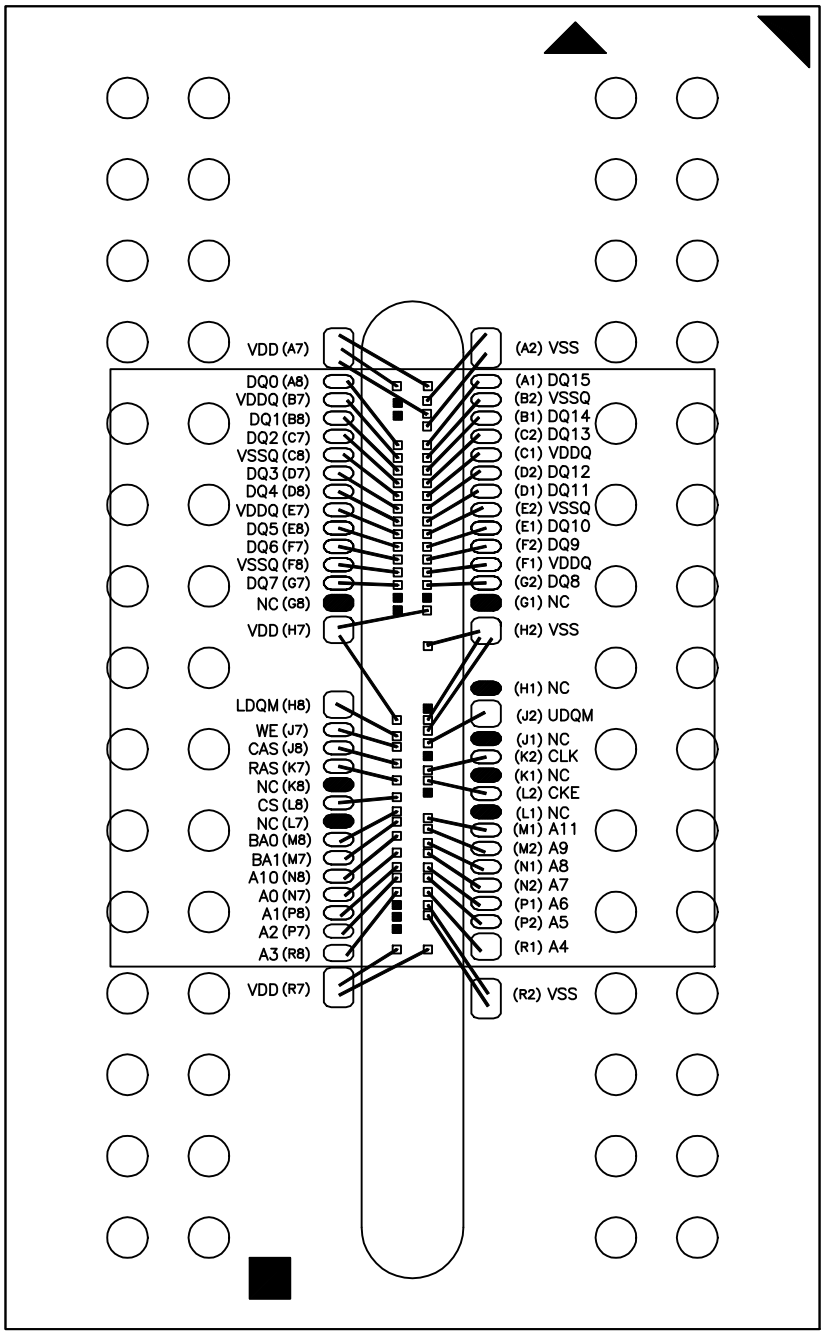
SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

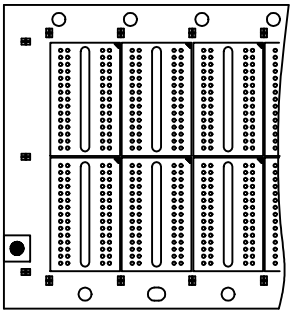
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

從VSS開始銲線
Start from VSS

Approved By

SDR SDRAM (x16)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 60
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
8Mx16 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/19/2001	12/19/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. MV060CD1012A

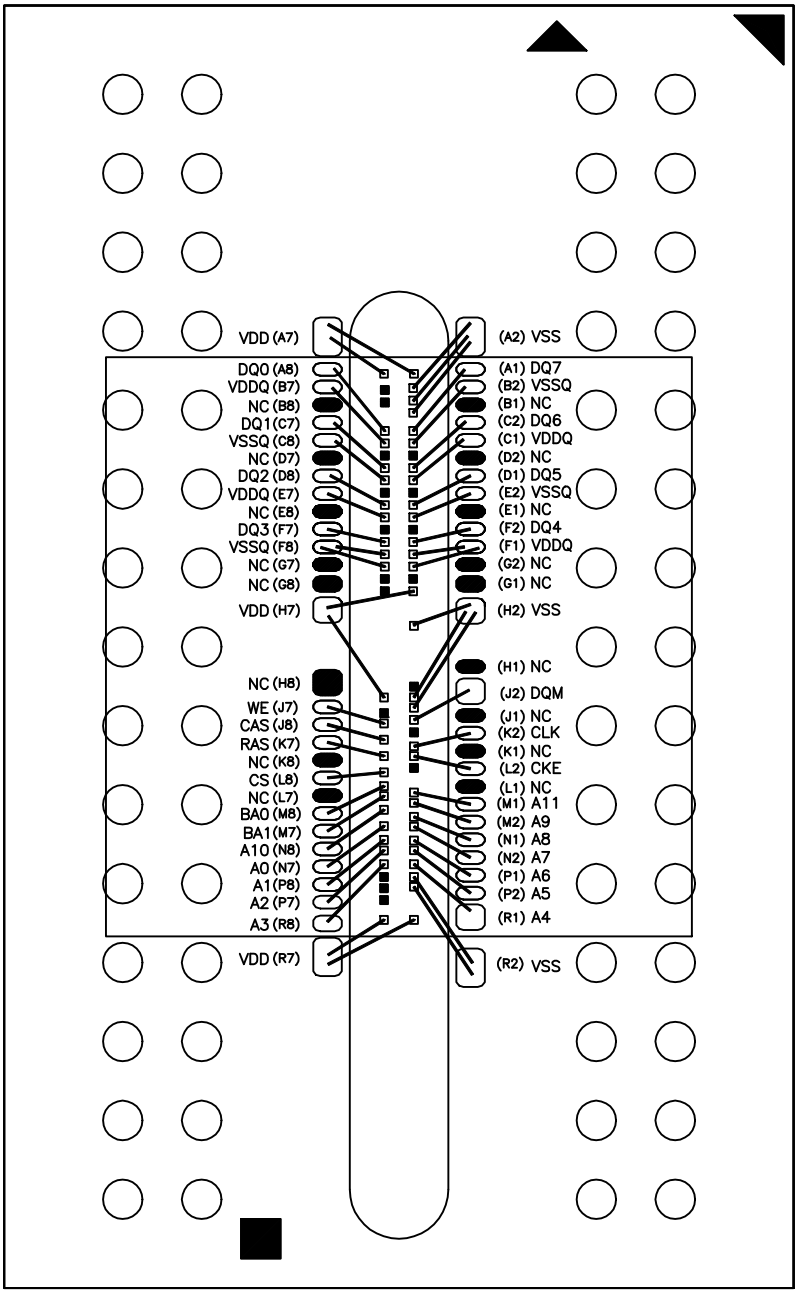
SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

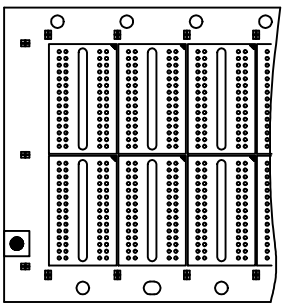
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

從VSS開始銲線
Start from VSS

Approved By

SDR SDRAM (x8)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 53
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
16Mx8 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/19/2001	12/19/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1011A

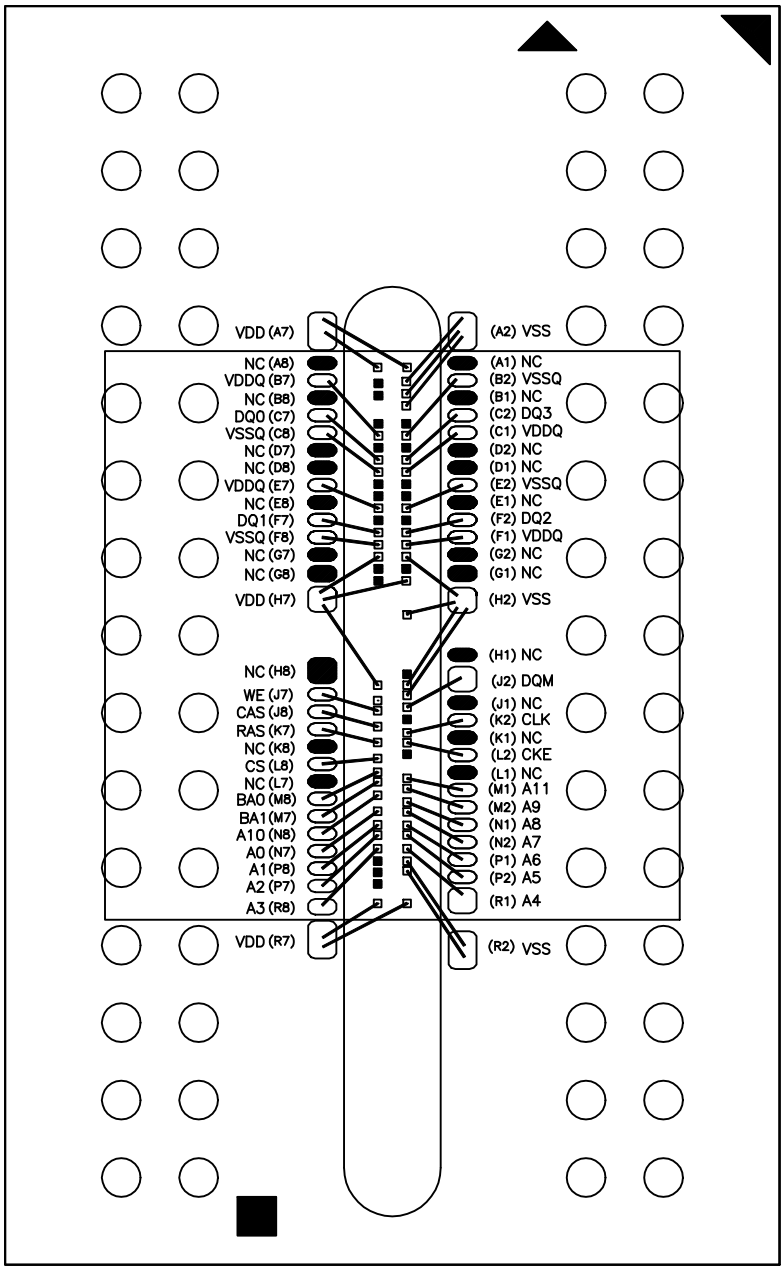
SERIES NO. | SCALE 14:1 | VER. | PAGE 1/1

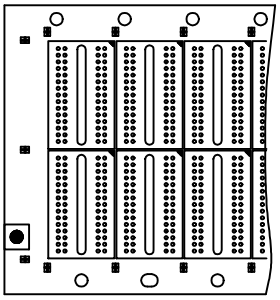
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

從VSS開始銲線
Start from VSS

Approved By

SDR SDRAM (x4)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 49
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
32Mx4 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/120/2001	12/20/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1010A

SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

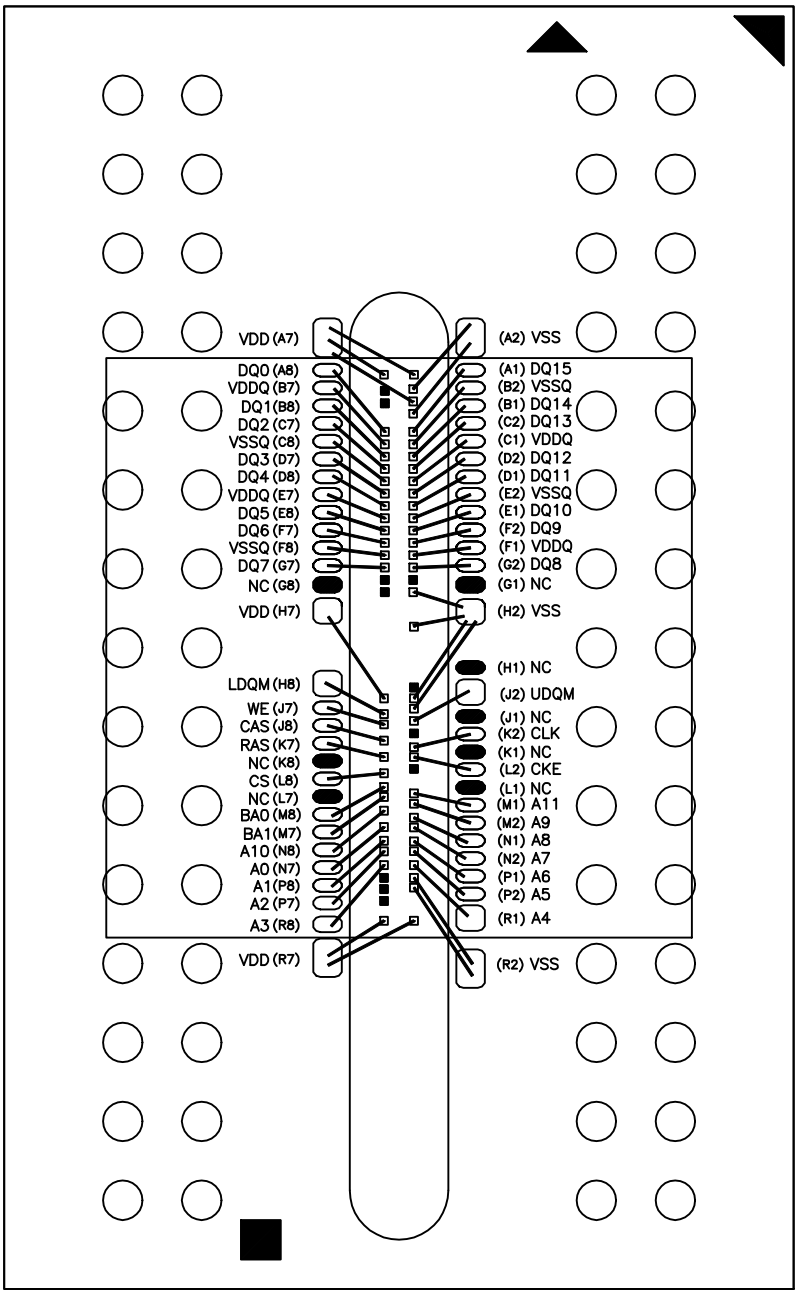
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

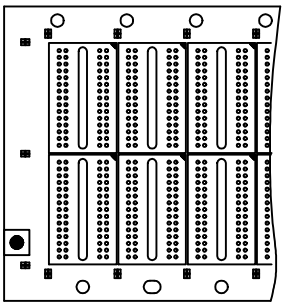
從VSS開始銲線
Start from VSS

Approved By

(LOW POWER)

SDR SDRAM (x16)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 60
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
8Mx16 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/20/2001	12/20/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1015A

SERIES NO. | SCALE 14:1 | VER. | PAGE 1/1

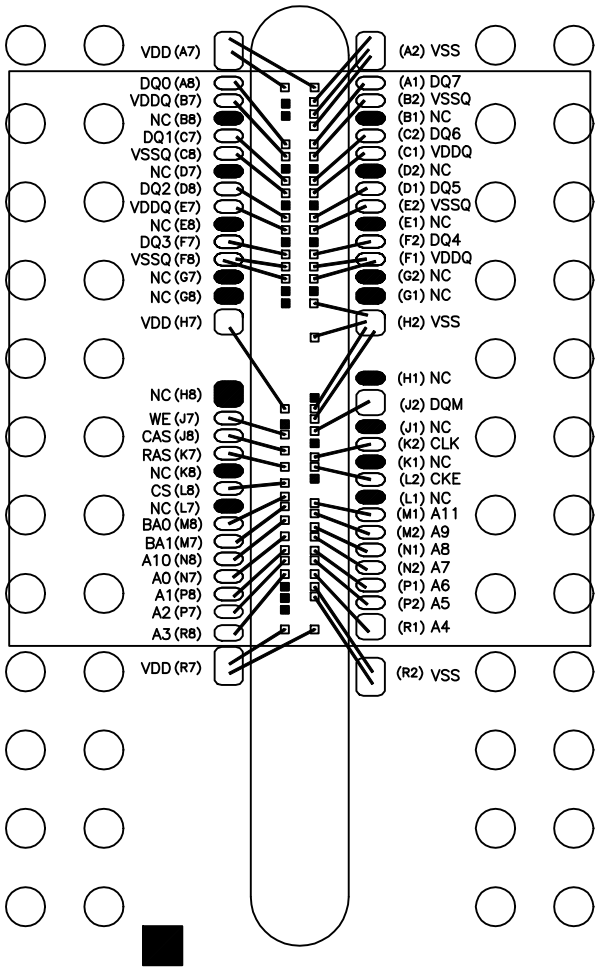
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

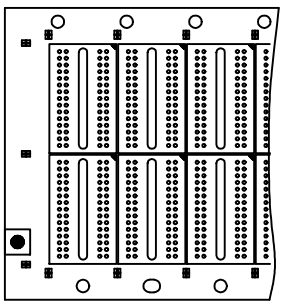
從VSS開始銲線
Start from VSS

Approved By

(LOW POWER)

SDR SDRAM (x8)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 53
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
16Mx8 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/19/2001	12/19/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV060CD1014A

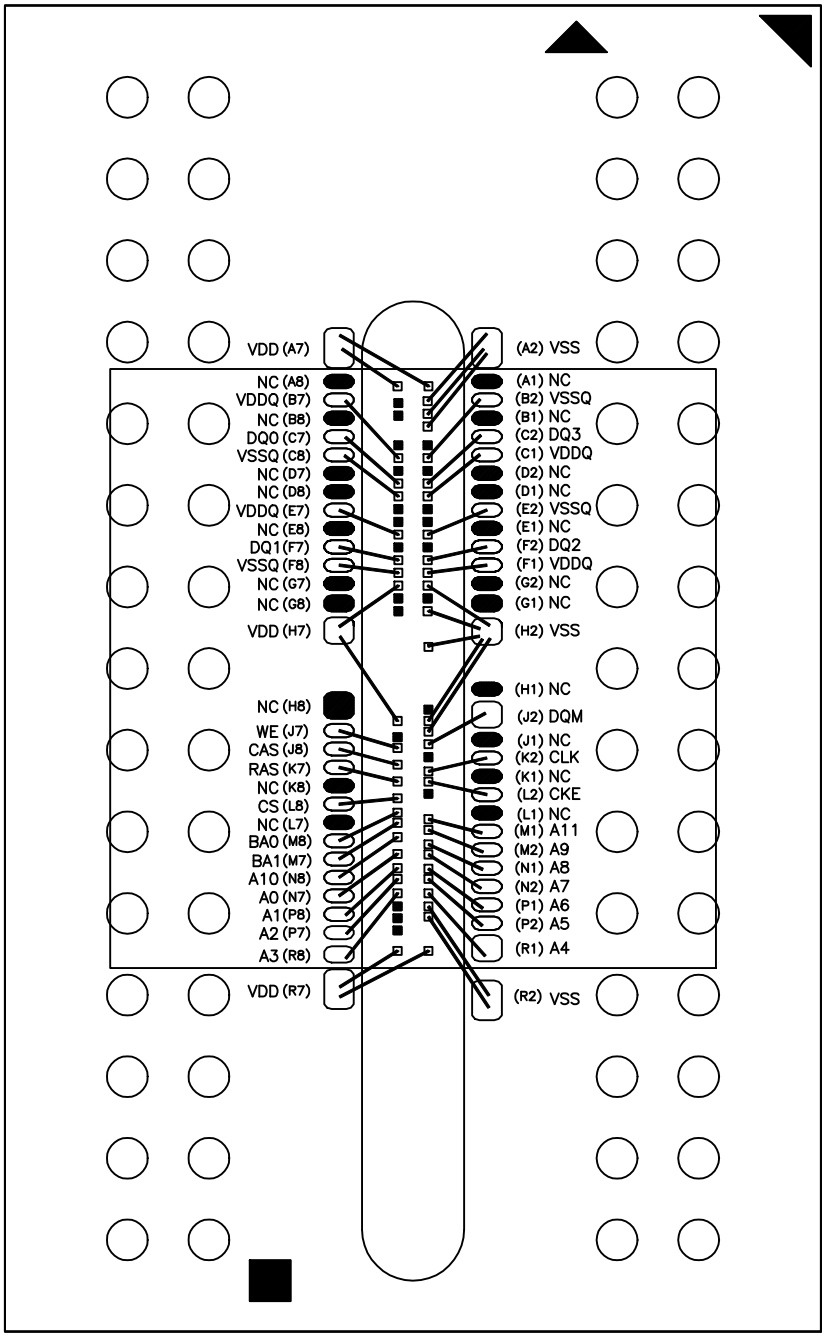
SERIES NO. | SCALE 14:1 | VER. | PAGE 1/1

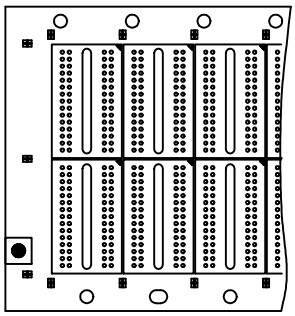
THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc..

從VSS開始銲線
Start from VSS

Approved By

(LOW POWER)
SDR SDRAM (x4)





CUSTOMER	: MV
SUB PACKAGE CODE	: CD060.01
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um(1.0mil)
CHIP COATING	: NO
WIRE PULL	: C7,C8,C1,C2,F7,F2,L8,L2,K7,K2
SUBSTRATE MATERIAL	: BT
WIRE AMOUNT	: 49
REMARKS	: Max wire length is 1.15mm(45mil)
	: Min bond pad opening is 80um
	: Min bond pad pitch is 100um

TITLE
60L SOC (8mmx13mm)
MOSEL-128MB(0.14um)
32Mx4 (128MB) SDRAM
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	Y.C. Chen	Vincent Tu		
DATE	12/20/2001	12/20/2001		

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

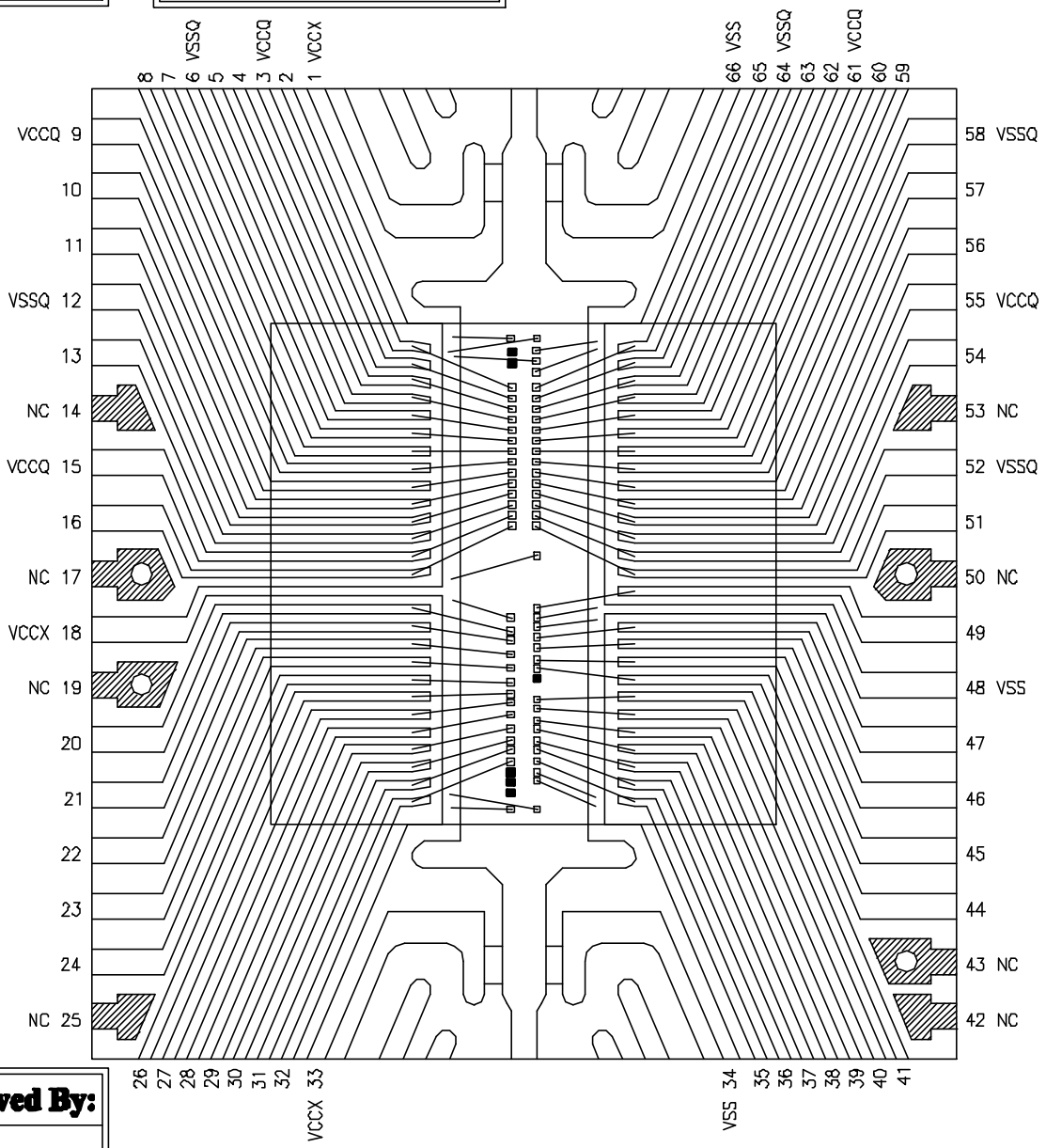
DWG NO. TDMV060CD1013A

SERIES NO.	SCALE	VER.	PAGE
	14:1		1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

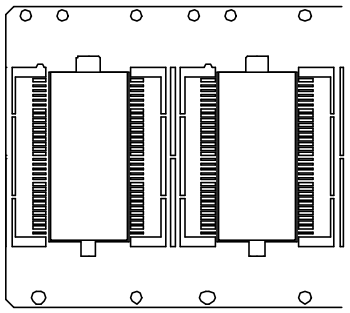
從 VSS 開始銲線
Start from VSS

Engineering Evaluation



Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA066
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,3,16,31,32,35,36,51,64,65
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 65
REMARKS	: MAX WIRE LENGTH IS 1.30mm (51mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
66L TSOPII (400x875mil^2)
128MDDR
8Mx16 DDR (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

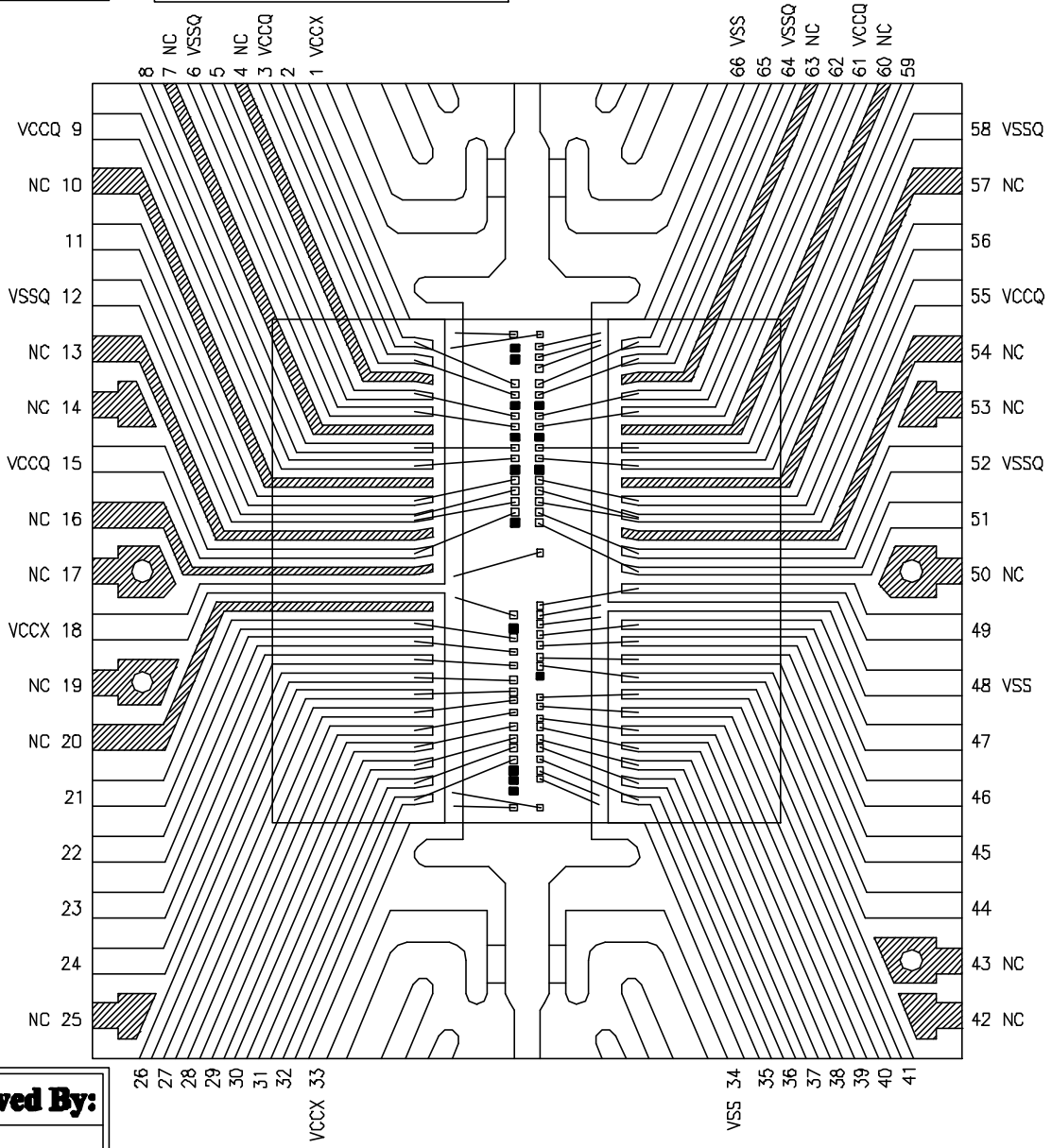
DWG NO. TDMV066TA1010A

SERIES NO.	SCALE	VER.	PAGE
	12:1	B	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

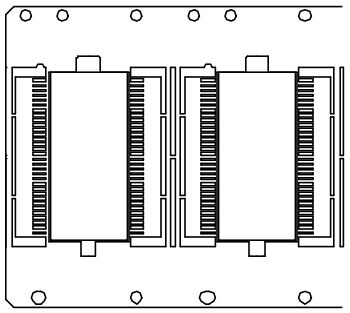
從 VSS 開始銲線
Start from VSS

Engineering Evaluation



Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA066
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,3,16,31,32,35,36,51,64,65
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 57
REMARKS	: MAX WIRE LENGTH IS 1.30mm (51mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
66L TSOPII (400x875mil^2)
128MDDR
16Mx8 DDR (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

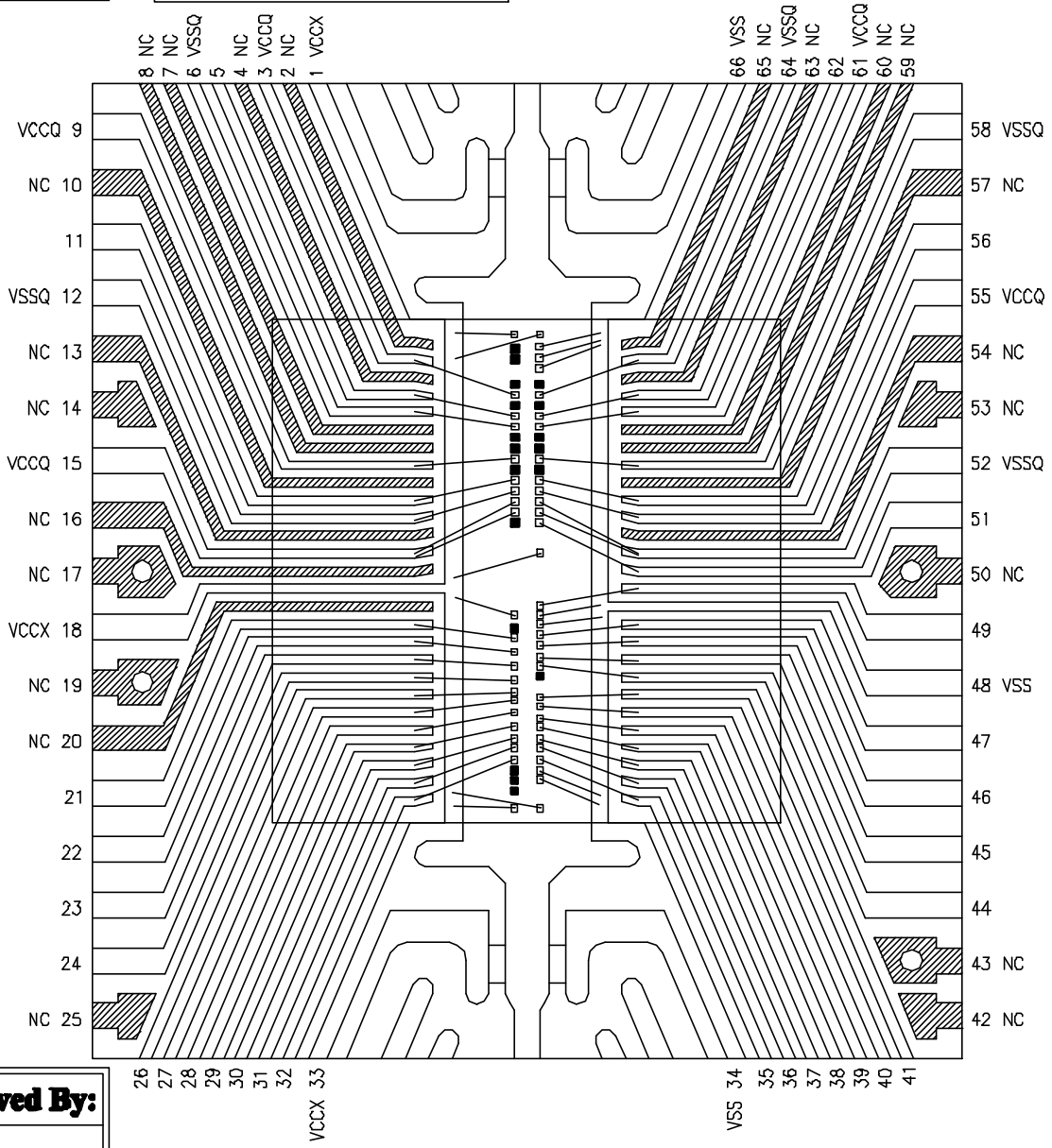
DWG NO. TDMV066TA1011A

SERIES NO.	SCALE	VER.	PAGE
	12:1	B	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

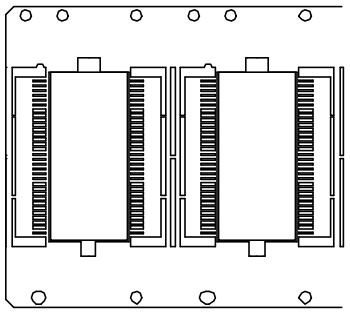
從 VSS 開始銲線
Start from VSS

Engineering Evaluation



Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA066
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,3,16,31,32,35,36,51,64,65
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 53
REMARKS	: MAX WIRE LENGTH IS 1.30mm (51mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
66L TSOPII (400x875mil^2)
128MDDR
32Mx4 DDR (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

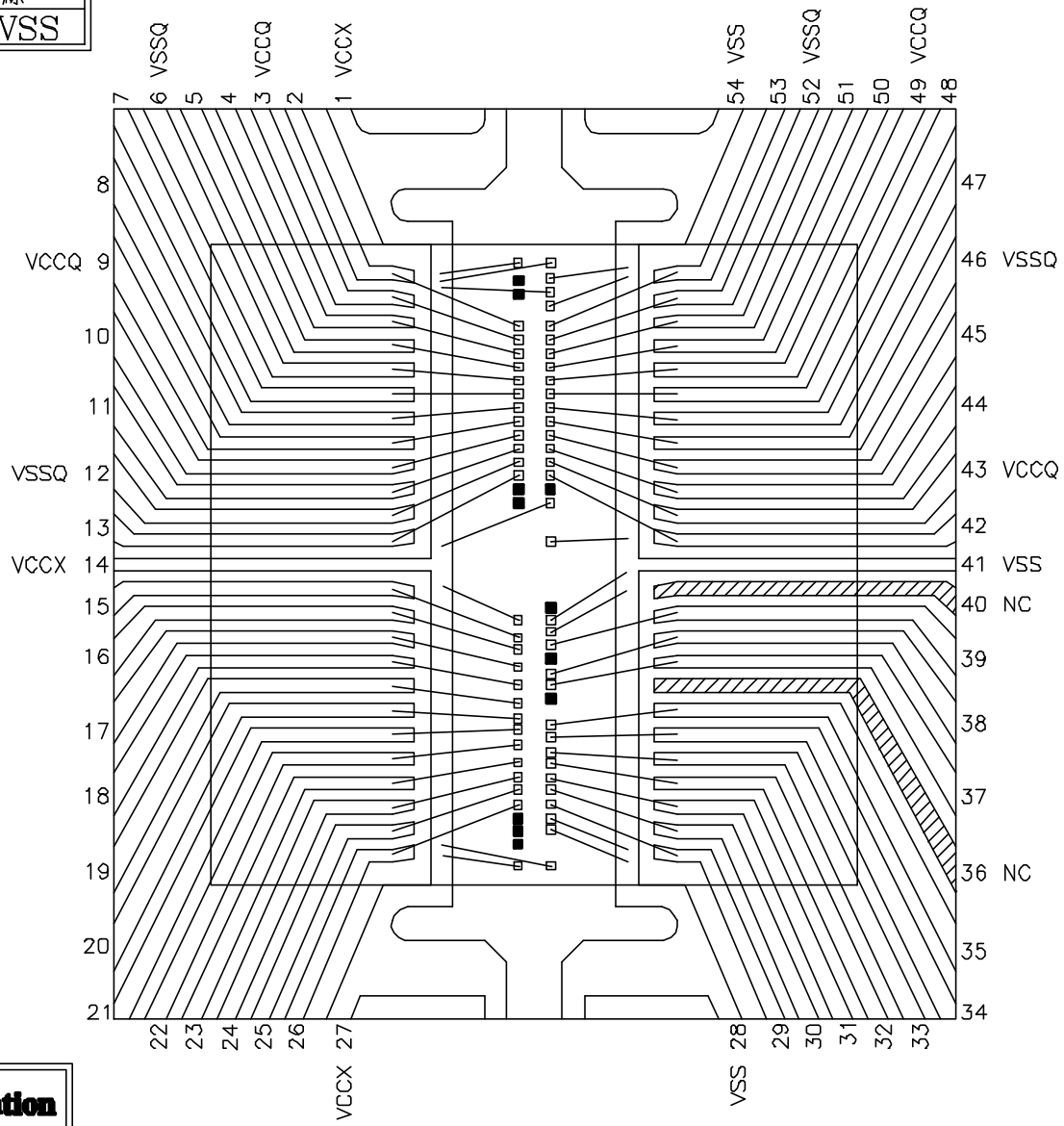
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV066TA1012A

SERIES NO.	SCALE	VER.	PAGE
	12:1	B	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

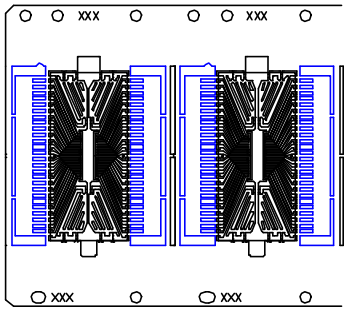
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA054
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,13,15,25,26,29,30,39,42,53
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 60
REMARKS	: MAX WIRE LENGTH IS 1.31mm (52mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil^2)
128M SDRAM
8Mx16 SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

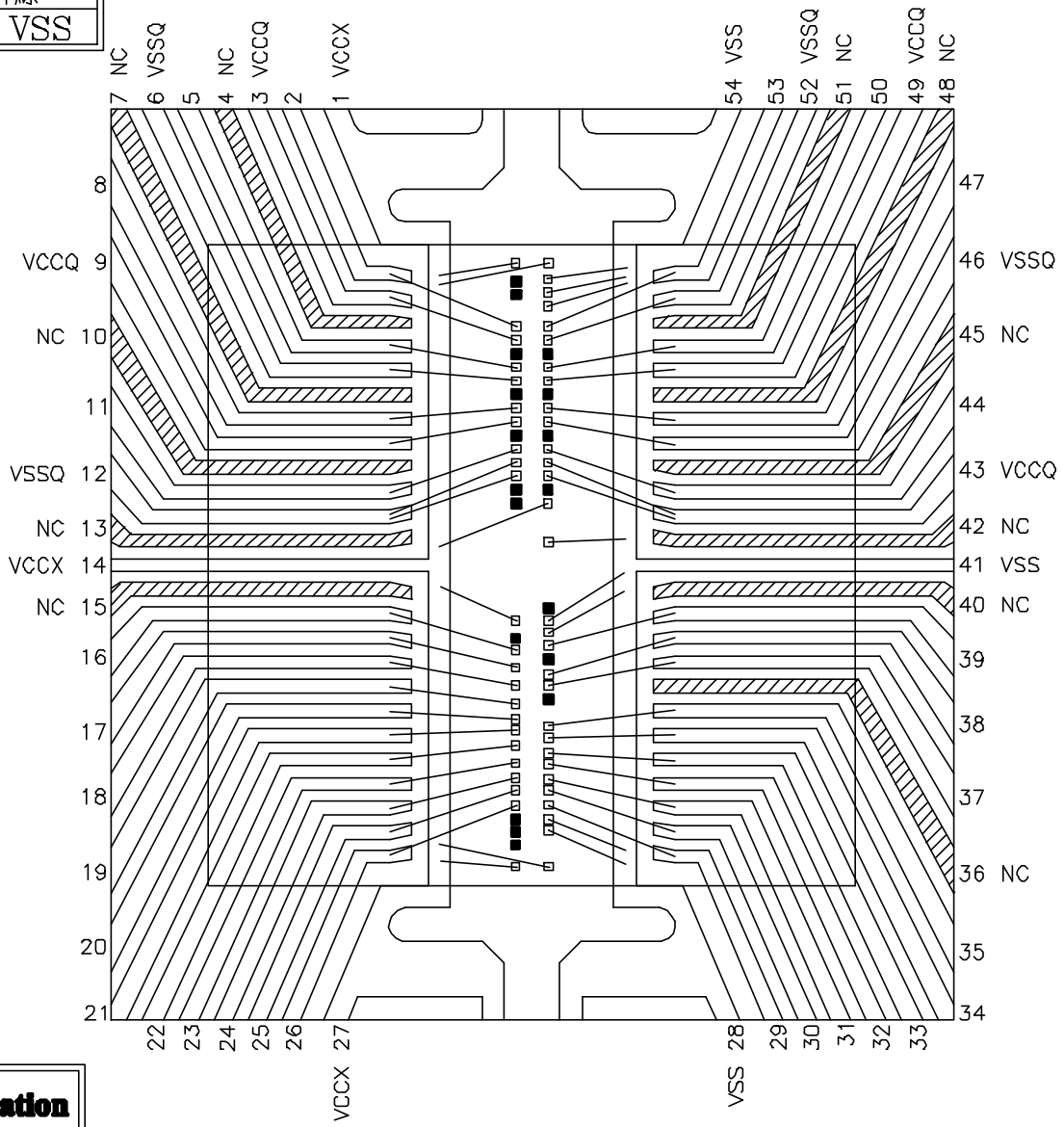
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1028A

SERIES NO.	SCALE	VER.	PAGE
	15:1	A	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

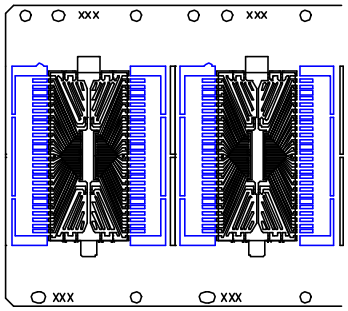
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA054.
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,12,16,25,26,29,30,39,43,53
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 53
REMARKS	: MAX WIRE LENGTH IS 1.26mm (50mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil^2)
128M SDRAM
16Mx8 SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

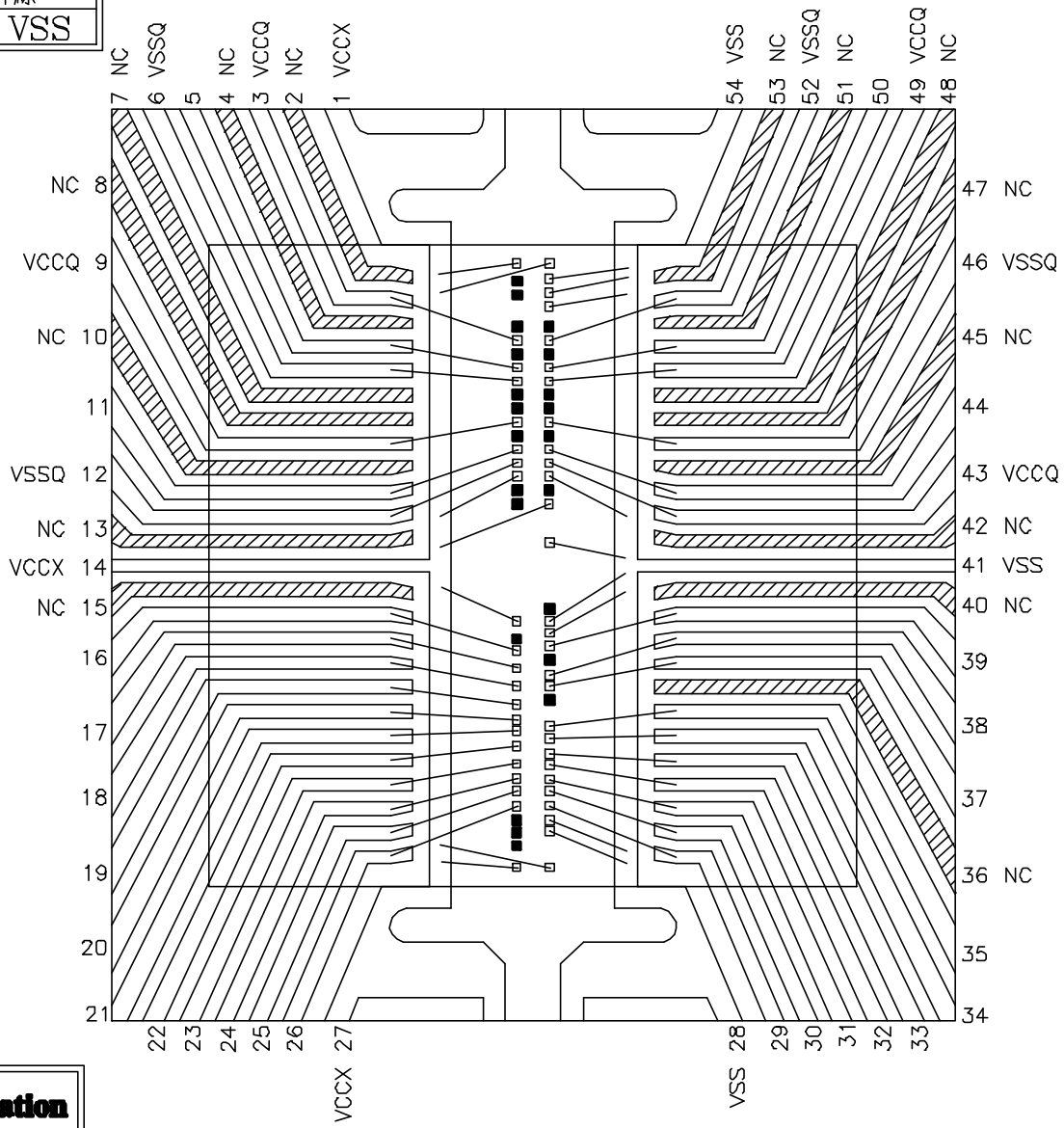
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1027A

SERIES NO. | SCALE 15:1 | VER. A | PAGE 1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

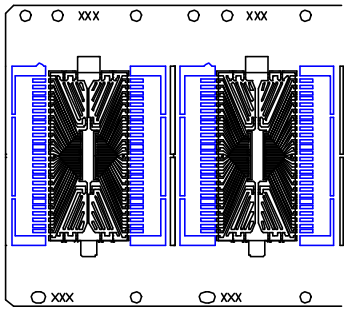
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI
SUB PACKAGE CODE	: NA
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm² (234x231mil²)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 3,12,16,25,26,29,30,39,43,52
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 49
REMARKS	: MAX WIRE LENGTH IS 1.27mm (50mil)
	: MIN BOND PAD OPENING IS 80x80um²
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil²)
128M SDRAM
32Mx4 SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

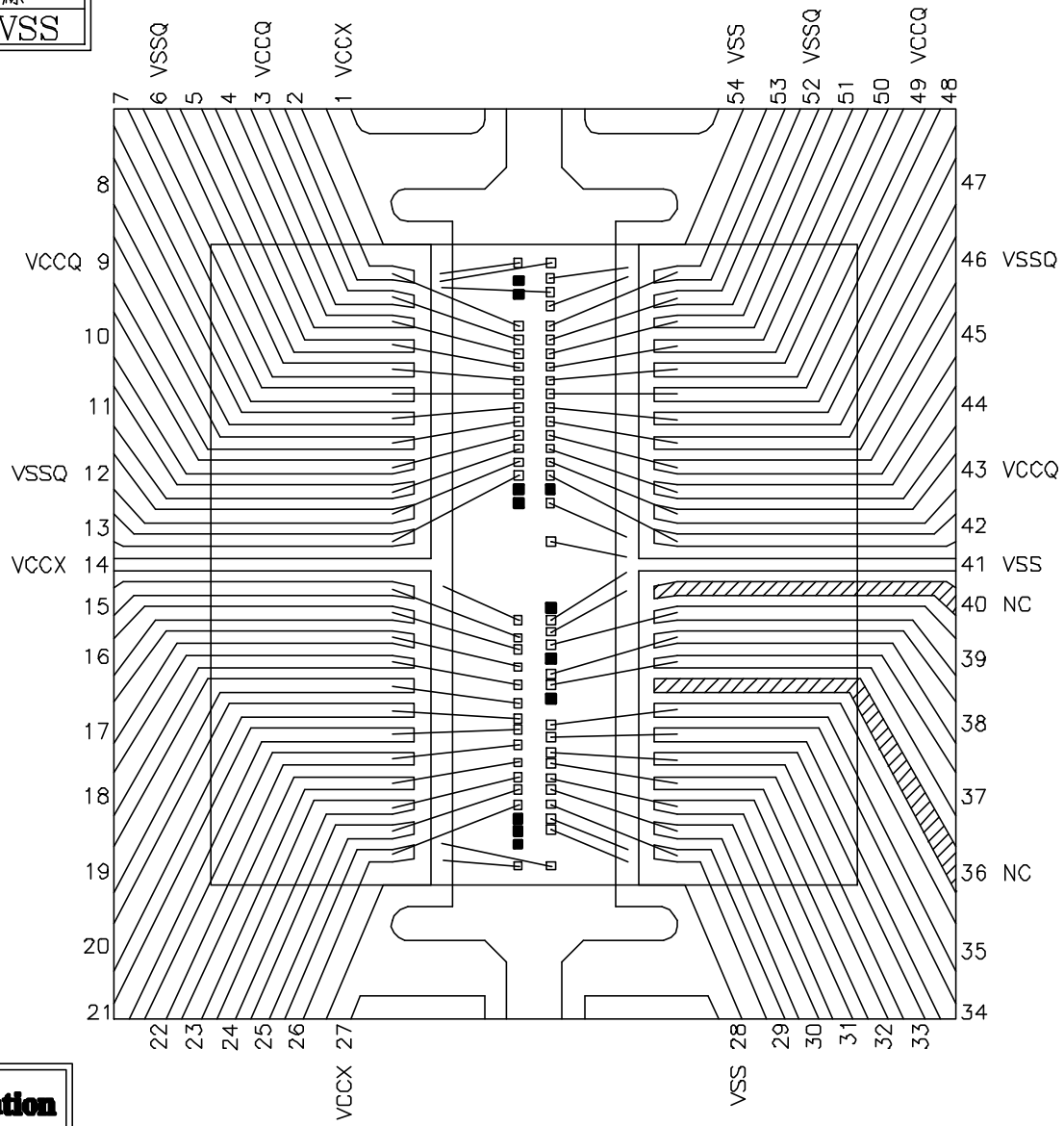
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1026A

SERIES NO.	SCALE	VER.	PAGE
	15:1	A	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

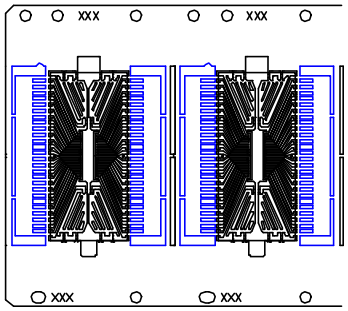
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA054
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,13,15,25,26,29,30,39,42,53
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 60
REMARKS	: MAX WIRE LENGTH IS 1.31mm (52mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil^2)
128M LPSDRAM
8Mx16 LOW POWER SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

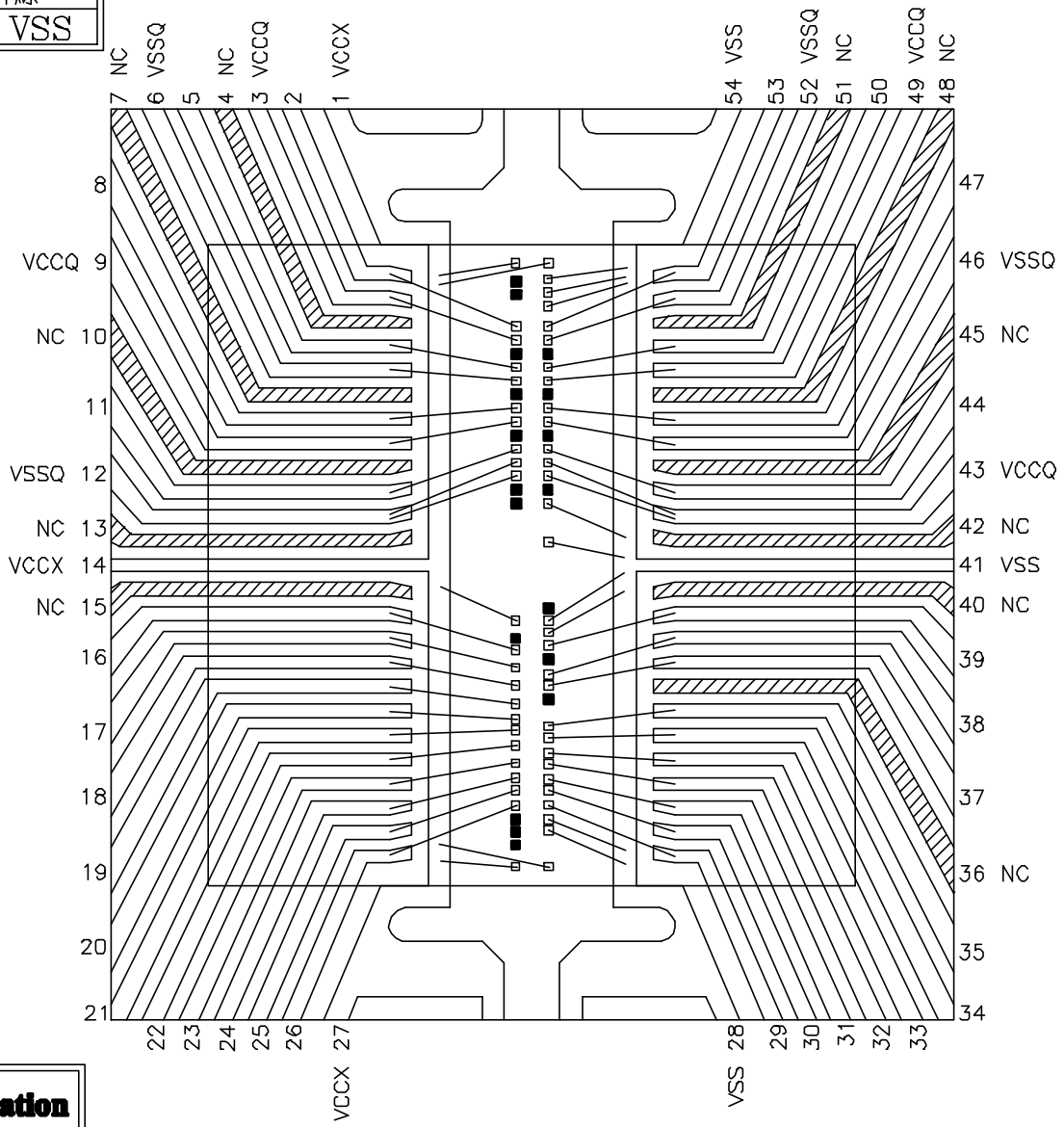
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1031A

SERIES NO.	SCALE	VER.	PAGE
	15:1	A	1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

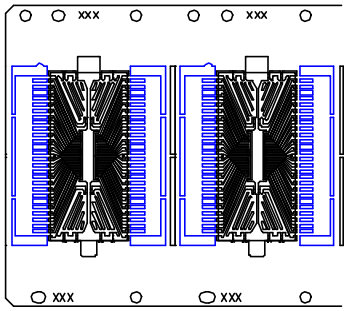
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA054
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm² (234x231mil²)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 2,12,16,25,26,29,30,39,43,53
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 53
REMARKS	: MAX WIRE LENGTH IS 1.26mm (50mil)
	: MIN BOND PAD OPENING IS 80x80um²
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil²)
128M LPSDRAM
16Mx8 LOW POWER SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

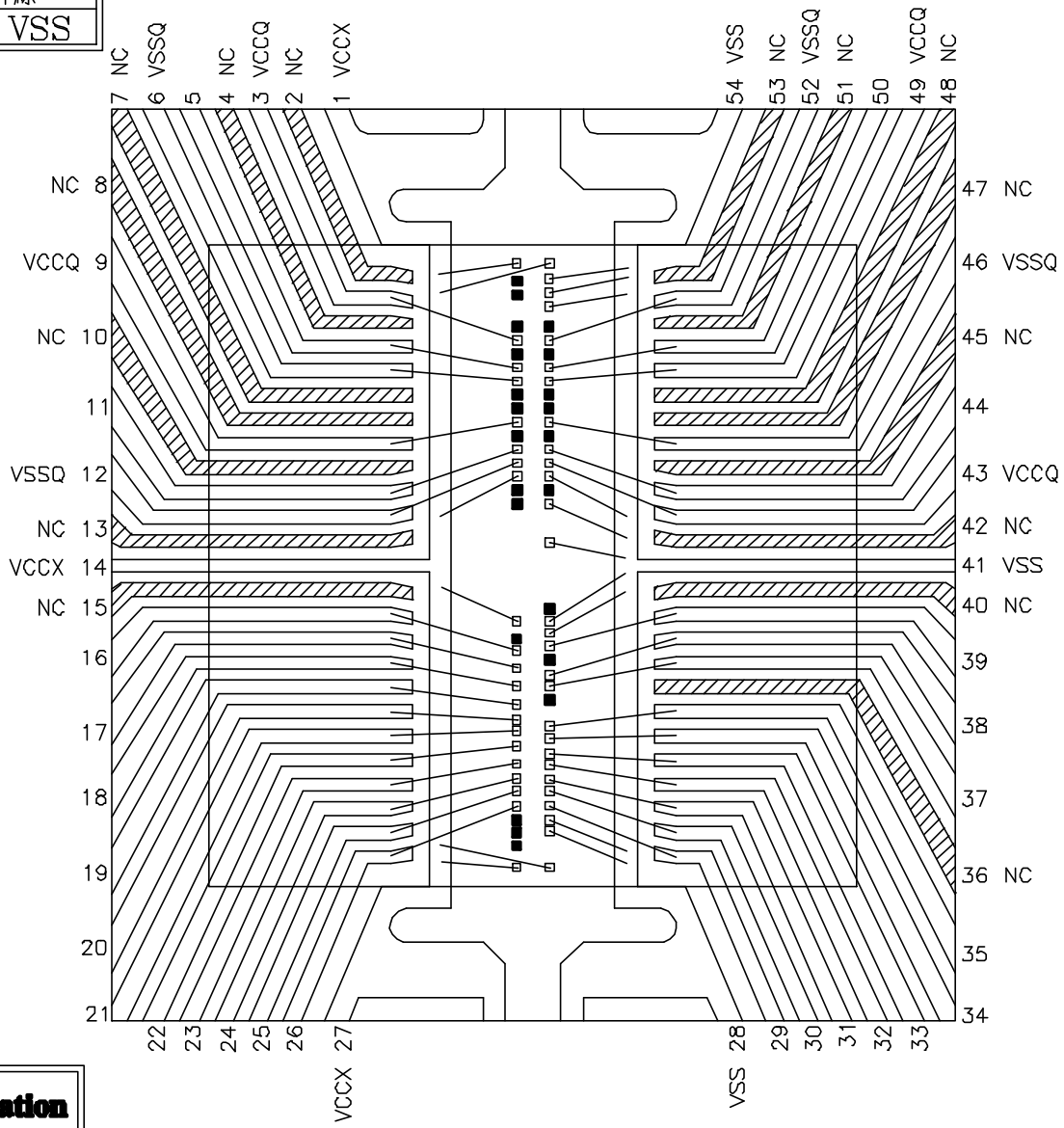
南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1030A

SERIES NO. | SCALE 15:1 | VER. A | PAGE 1/1

THE INFORMATION CONTAINED HERE IN IS THE EXCLUSIVE PROPERTY OF ChipMOS Technologies Inc. AND SHALL NOT BE DISTRIBUTED, REPRODUCED, OR DISCLOSED IN WHOLE OR IN PART WITHOUT PRIOR WRITTEN PERMISSION OF ChipMOS Technologies Inc.

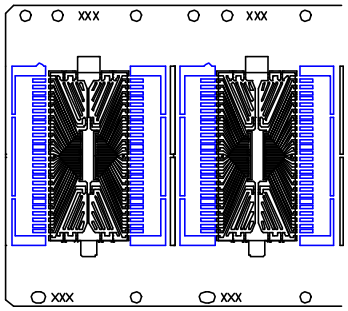
從 VSS 開始銲線
Start from VSS



Engineering Evaluation

Customer Approved By:

PIN1



CUSTOMER	: MVI (MV)
SUB PACKAGE CODE	: TA054
DIE PAD DIMENSIONS	: LOC TYPE (2323)
DIE DIMENSIONS	: 5.937x5.872mm^2 (234x231mil^2)
WIRE AU	: 25um (1.0mil)
CHIP COATING	: NO
WIRE PULL	: Pin 3,12,16,25,26,29,30,39,43,52
LEADFRAME MATERIAL	: A42
WIRE AMOUNT	: 49
REMARKS	: MAX WIRE LENGTH IS 1.26mm (50mil)
	: MIN BOND PAD OPENING IS 80x80um^2
	: MIN BOND PAD PITCH IS 100um

TITLE
54L TSOPII (400x875mil^2)
128MLPSDRAM
32Mx4 LOW POWER SDRAM (0.14um)
BONDING DIAGRAM

	DRAWN	DESIGNED	CHECKED	APPROVED
BY	H.W. CHEN	H.P. LIU	VINCENT TU	M.L. HUANG
DATE	12/21/2001	12/21/2001	12/21/2001	12/21/2001

南茂科技股份有限公司
ChipMOS TECHNOLOGIES INC.

DWG NO. TDMV054TA1029A

SERIES NO.	SCALE	VER.	PAGE
	15:1	A	1/1

128D14 PAD COORDINATES

128D14 PAD COORDINATES (final)				01/15/2002
No Shrink				
Coordinates are in relation to "chip" cell (center origin)				
ze = 73.4x73.4um, C2 Size = 70.8x70.8um				
= 5768 um (to seal ring metal2 extent)				
= 5833 um (to seal ring metal2 extent)				
PAD NAME	X-COORDINATE	Y-COORDINATE	RPAD	
			PROBE	
VCCX	-2767.72	152.12	NO	
VBLEQ	-2567.07	152.12	YES	
VBLH	-2447.07	152.12	NO	
VPP	-2332.07	152.12	YES	
APAD<3>	-2202.87	152.12	NO	
APAD<2>	-2062.85	152.12	NO	
APAD<1>	-1957.05	152.12	NO	
APAD<0>	-1817.03	152.12	YES	
APAD<10>	-1652.03	152.12	YES	
BAPAD<1>	-1512.01	152.12	NO	
BAPAD<0>	-1412.01	152.12	NO	
CSBPAD	-1271.99	152.12	YES	
RASBPAD	-1106.99	152.12	YES	
CASBPAD	-941.99	152.12	YES	
WEBPAD	-776.99	152.12	YES	
LDMPAD	-671.86	152.12	NO	
VCCX	-513.23	152.12	YES	
DQSPAD<0>	562.89	143.62	NO	
VCCQ	687.89	143.62	NO	
DQPAD<7>	812.89	143.62	YES	
VSSQ	937.89	143.62	NO	
DQPAD<6>	1062.89	143.62	YES	
DQPAD<5>	1187.89	143.62	NO	
VCCQ	1312.89	143.62	YES	
DQPAD<4>	1437.89	143.62	NO	
DQPAD<3>	1562.89	143.62	NO	
VSSQ	1687.89	143.62	NO	
DQPAD<2>	1812.89	143.62	YES	
DQPAD<1>	1937.89	143.62	NO	
VCCQ	2062.89	143.62	NO	
DQPAD<0>	2187.89	143.62	NO	
VBB	2477.98	143.62	YES	
VINT	2602.98	143.62	NO	
VCCX	2767.72	152.12	NO	
VCCX	2767.72	-152.12	NO	
VSS	2621.90	-143.62	NO	
X16PAD	2496.90	-143.62	YES	
VSS	2371.90	-143.62	NO	
DQPAD<15>	2187.89	-143.62	NO	
VSSQ	2062.89	-143.62	NO	
DQPAD<14>	1937.89	-143.62	NO	
DQPAD<13>	1812.89	-143.62	YES	
VCCQ	1687.89	-143.62	NO	

128D14 PAD COORDINATES

DQPAD<12>	1562.89	-143.62	NO	
DQPAD<11>	1437.89	-143.62	NO	
VSSQ	1312.89	-143.62	YES	
DQPAD<10>	1187.89	-143.62	NO	
DQPAD<9>	1062.89	-143.62	YES	
VCCQ	937.89	-143.62	NO	
DQPAD<8>	812.89	-143.62	YES	
VSSQ	687.89	-143.62	NO	
DQSPAD<1>	562.89	-143.62	NO	
DDRPAD	213.12	-152.12	NO	
VREFPAD	-402.27	-152.12	NO	
VSS	-513.23	-152.12	YES	
VSS	-618.45	-152.12	NO	
UDMPAD	-741.27	-152.12	YES	
CLKBPAD	-867.84	-152.12	NO	
CLKPAD	-1007.86	-152.12	YES	
CKEPAD	-1107.86	-152.12	NO	
VNWL	-1227.86	-152.12	YES	
APAD<11>	-1477.01	-152.12	YES	
APAD<9>	-1582.26	-152.12	NO	
APAD<8>	-1722.28	-152.12	NO	
APAD<7>	-1822.28	-152.12	YES	
APAD<6>	-1962.30	-152.12	NO	
APAD<5>	-2062.30	-152.12	NO	
APAD<4>	-2202.32	-152.12	NO	
VSS	-2332.07	-152.12	YES	
VSS	-2432.07	-152.12	NO	
VCCX	-2767.72	-152.12	NO	

E – DATA SHEET (TARGETS AND KEY SPICE RESULTS)

Same as S17.

The following items are worth noting:

a) The QFC function is no longer implemented.

F – TEST MODES / MODE REGISTER

A description of the test modes is attached.

D14 128M Test Mode Descriptions

The entire Test Mode documentation is contained in this single D14TM#.xls file.
Several "sheets" within this file are ulitlized as follows: (#=revision number)

SHEET	**PURPOSE**
DESC	Main description of test mode document
REGISTERS	Details the bit assignment of the 3 test mode registers
SOFT SET INFO	Details how the Voltage Control Register handles each supply.
FUSE BLOW INFO	Details how the Voltage control fuses handle each supply
COUNT	Details on row and column count sequences in TMRPAD mode.
TMWLS	Most efficient activation scheme for wordline stressing, NOT for TMRPAD mode.
EX-1	Example of test using TMRPAD and RMW pattern
EX-2	Example of cell margin test
EX-3	Example of burn-in test
Revision	Revision history for D14 Test Modes
FAQs	Frequently Asked Questions

The test modes for the D14 128M have to be described in several parts.

a) Overall description of entire test mode system.
b) How to load the various test registers.
c) Description of each individual mode in the main register and how it works.
d) Detailed description of the voltage control registers and how they work.
e) Detailed description of the scramble control registers and how they work.
f) Detailed description of the reduced pad testing mode (redpad).

In general this is just a description of the test modes and how they operate.
The actual tests chosen for production/verification, and how they eventually
use these modes will have to be documented separately.

<A> Overall description of test mode system.

The D14 has many more test modes than the previous S17 parts designed by UMI. Also, the D14 chip loads and utilizes all the test modes in a fashion that is compatible with the redpad testing at wafer probe.
In addition to more test modes, all of the generated supplies and pumps have more fuse and soft set controls.
There are 3 registers that contain the test mode information.
These registers are loaded serially with 4-bit wide words.
(The words are only 4-bits wide to accommodate redpad testing.)
The loading sequence of these registers is a little complicated and is explained in section <B>.

Test Register #1, the main test mode control register, is 7 bits deep by 4 bits wide. (7x4=28 total bits.) These bits correspond directly to a particular test mode. Currently there are 25 test modes implemented (3 open bits).
Section <C> will describe each of these modes in detail.

Test Register #2, the voltage set register (VSR) is 8 bits deep by 4 bits wide.
Each 4-bit word in this register controls a particular voltage supply or pump (except VREF and VRAT which share a 4-bit word with 2-bits each).
The voltage control register can be used independently from any of the test modes in the main test register.
Note, this design has no set test modes for burn-in (i.e.TMPKBI, or TMACBI)
To implement the desired voltages for a particular burn-in condition, just set each of the supplies according to the voltage set registers.
In each case, if a 4-bit word in the register is left as "0000", that corresponds to the default condition and the particular supply is not modulated.
Section <D> contains all the details on setting these registers and using them.

Test Register #3, the "Scramble Control" register, controls the data pattern for compression testing (TMCOMP mode). In TMCOMP mode, the data written to the part comes from the internal data generator, not the tester.
During compression reads, the read data is compared with the data generator to make sure it matches (=pass, "1") or not (=fail, "0").
The 4-bit x 4 scramble register changes the data based on X and Y addresses to give the desired topological pattern. The read data can also differ from the write data for a particular pattern to facilitate Read-modify-write functions. Section <E> contains all the details on using the scramble for data generation.

Section <F> describes redpad testing in detail. Redpad can be entered in 2 ways.
1) By IO configuration X16VCC=0 DQ8=0 DQ7=0
2) By accessing the TMRPAD bit in the main test register.

Accessing the redpad mode from a package (method #2) will be critical for analyzing fails after packaging. The need to go back and see if a bit passes or fails the original wafer test is used quite a lot.

All the test modes are accessed the same way for both redpad and normal mode. This will keep a lot of the test code identical for wafer and package testing.

Some modes and functions are fixed in redpad mode and can't be changed.
e.g. The part will be DDR, BL=2, CL=2, and the TMCOMP mode must be used.
The DLL will be off, the DQS pins are not needed.
VREF is generated internally and is not to be probed.

The CAS/RAS/WE pins are required. The CSB pin is presently required, but it can be held at ground (0V) with no need for a driver channel.

Only A11/A10/A7/A0 are used for address pins. However, they do not control any direct row or column addressing. Their main purpose is to load the registers and provide the switches necessary in controlling special redpad functions.

DQs 2,6,9,and 13 are used for reading data.
The UDM pad is used to measure voltages (with some possibility of slight error).
VINT, VBLH, VPP, VBB, VNWL, and VBLEQ can also be measured and/or forced directly since they have dedicated test pads.

<B> How to load the various test registers

see sheet "REGISTERS" for examples.

The loading of these registers is somewhat complicated.
This is for two reasons, first it has to be accessible in redpad mode,
secondly, to avoid accidental access by a user it has to be hard
to enter.
The old S17 register was loaded with a single mrs command using
A7=1. This is now impossible since A7 has to be used as an input bit.

The basic sequence is this:
1) EMRS with A<2>=1 enable power to test buffers,
2) MRS with A<11,10,7,0>=1010 , load enable
3) MRS to select which register to load, see codes below
4) as many MRSs as needed to load desired register, A<11,10,7,0>=data
5) issue non-mrs to cancel loading
6) repeat steps 2-5 if another register is to be loaded
7) MRS with A<11,10,7,0>=1111 to enable the modes
(MRS with A<11,10,7,0>=1110 can disable the modes at any time
without dumping the register contents.)
(a normal MRS also does this function)

reset) MRS with A<11,10,7,0>=010x resets all the test mode bits in all
3 registers and of course disables them.

**If you want to change the normal MRS configuration, while test modes
are active, then A<11,10,7> must all be "0" to avoid resetting.

Details of loading test registers:

STEP

#1 Set TMPEN=1, Test Mode Power Enable, EMRS with A<2>=1

This step enables all the test address buffers. To save power, they are disabled unless this step is performed.

(This step can be skipped if already in redpad mode via the IO configure method. EMRS commands can't be given in redpad mode.)

#2 MRS, Load Enable

A <11>	<10>	<7>	<0>
1	0	1	0

after a load enable, only MRS commands can be issued to preserve the load sequence. Any non-mrs command will terminate the loading.

#3 MRS, Register select

A <11>	<10>	<7>	<0>	(pick one)
0	0	1	1	main test register (MTR)
0	1	1	1	XY scramble register (XY)
1	0	1	1	voltage set register (VSR)

#4 MRS, Register load steps

Load the selected register serially, keeping the commands in MRS mode. Use A<11,10,7,0> to program the selected bits.

The attached tables (sheet "REGISTER") indicate the bit assignment of each register.

Provide as many cycles as necessary to the load the register.

Main test register =	7 cycles	table TM-D-1
XY scramble register =	4 cycles	table TM-D-2
Voltage set register =	8 cycles	table TM-D-3

**Note for advanced users, the registers load from the bottom up. This is so the source code for the tester can be easily matched with the tables in documentation. This means if only a particular row in the register is to be loaded, you only need enough clock cycles to get that high in the stack. The master reset can be used prior to loading to ensure all other bits remain at the "0" state. Example, just loading TMSCLK would require 5 cycles (load from bottom up!).

#5 Cancel Loading - issue non-mrs to cancel the loading (NOP suggested)

#6 Repeat steps 2-5 if another register is to be loaded.

#7 MRS, enable the test modes

A <11>	<10>	<7>	<0>
1	1	1	1

Simply loading the registers doesn't enable the modes. One more level of protection is achieved by requiring this enable command. Plus, modes can't be executed as they "shift" through during the load sequence.

<disable>	MRS, disable the test modes	A <11>	<10>	<7>	<0>
		1	1	1	0

This disables the modes, but does not destroy the register contents.
A normal MRS also does this function, again for protection in a normal use environment.

<reset>	MRS, reset all	A <11>	<10>	<7>	<0>
		0	1	0	x

This resets the contents of all test registers and disables them.
TMPEN must be enabled for this function to work (EMR<2>).

If issuing normal MRS commands while test modes are active, make sure A<10>=0 to avoid this master reset!!!

**A "reset all" can be issued even if the test modes have been disabled.

The key difference is that the reset destroys the contents of all 3 test registers and resets them to "0". No test modes can be active from that point.

The "disable" feature deactivates the test modes by ignoring the register contents, but since they are not destroyed, they can be reactivated again.

C) Detailed description of the main test modes and how they work.

**There are a number of test modes and test signals that do not correspond directly to bits in the MTR (eg. TMINV), they are described in detail in the TMRPAD section (F)-"Extended Commands/Modes".

TM<#>	TM SIGNAL	Description
0	TMVMEAS	Enables the UDM pad to measure DC voltages. (lvs=TM<0>) The voltage to be measured depends upon the state of TM<3,2,1> When this mode is used, masking is disabled (for both LDM and UDM). These voltages should be measured with a very high impedance volt-meter since we cannot source a lot of current through these measure paths. Some amount of calibration may be necessary. True VBLH, VINT, and VPP pads exist to perform this calibration on.
3,2,1	TM<3,2,1>	Decode to determine what voltage is measured in TMVMEAS mode TM <3> <2> <1> 0 0 0 VPL 0 0 1 VREF 0 1 0 VBLH 0 1 1 VINT 1 0 0 (open) 1 0 1 VBLEQ 1 1 0 VPP/2 1 1 1 (open)
4	TM4BK	4 bank active and write mode. When this bit is enabled, all active and write commands go to all four banks in parallel. The same row address is valid in all four banks. For writing, the same column and data will be used. You do not have to be in TMCOMP mode to use this. You do not have to be in TMREDPAD mode to use this.
5	TMRAS	This mode defeats the ras inter-lock timer and the automatic precharge in refresh cycles. So it has two uses. First, you can find the true TRAS by defeating the interlock. Secondly, for refresh cycles, you can read and write to the array after the refresh timer would have expired (~80ns should be safe). This method was used in the past to verify the refresh counter, and it still could, but there are other methods available now since the refresh counters can be reset and have a known starting point.
6	TMCBRSHT	This mode shortens the refresh timer by about 4ns. The tras time is shortened directly, which then reduces trfc as well It may be useful in finding marginal bits under the refresh conditions. See CONBLK/REFDEL schematic for details.
7	TMCBRUP	This mode slaves the wordline high time to the external clock high time This is useful for burn-in, so REF cycles can be executed with the wordlines high for nearly the entire time (equal to the duty cycle). See CONBLK/REFCLK circuit for details

8	TMCKE0	This mode allows CKE to be low in redpad mode. (ie this mode can't be used unless TMRPAD is active) When this mode is activated, the CKE pad is actually equal to the opposite state of the WEBPAD. Note, CMOS levels should be used on the WEBPAD during this testing Note, WEBPAD is still doing it's normal functions as well, so the potential command space is somewhat limited. WEBPAD=1 for NOP, REF, and ACT commands so they can be used in a CKE=0 type power measure situation See CLKGEN/CKEBUF schematic for details.
9	TMSCLK	This is the slow clock test mode. The internal JCLK, and the following YCLK are "fixed" width pulses. This mode extends both of them JCLK is extended by about 3x, YCLK is extended by about 2.5: Of course the amount of extension varies by voltages and temperature. See CLKGEN/CLKDRV schematic for complete details.
10	TMRDEN	This is the redunancy test enable mode. In normal mode (non-redpad), the LDM pad will be the extended address that indicates whether to address a spare or not. In TMRPAD mode, if this is enabled, the row and column counters wil automatically count into the spares. The spare address for the rows is the MSB. Refered to as R<99> The spare address for the columns is the MSB. Referred to as C<99> The attached tables (in sheet "COUNT" if you have the .xls file open indicate the various counting sequences. TM-F-3,TM-F-4
11	(open)	No mode assigned to this bit.
12	TMA0<1>	This mode fixes the A0 row address="1". It is most useful for wafer level burn-in when all the odd wordlines need to be stressed at once. For this it should be combined with the TMWLS mode. Note-The row address counter is then decreased by a factor of 2. See RABLK/RABUF schematic for details. **DO NOT ACTIVATE TM 12 AND 13 AT THE SAME TIME.
13	TMA0<0>	This mode fixes the A0 row address="0". It is most useful for wafer level burn-in when all the even wordlines need to be stressed at once. For this it should be combined with the TMWLS mode. Note-The row address counter is then decreased by a factor of 2. See RABLK/RABUF schematic for details.
14	TMR11MS	For this mode the A11 Row address is the most significant in the counter. A10 row is the next most significant. (usually A11 is the LSB, A10 the next LSB) Note- If TMRDEN is set, the spare will be the most significant row address. This mode will be most useful for wafer test, then the rows will count in physical order and no scramble will be needed to match the tester with the TMRPAD row counter. There are times though (including normal operation) when the R11/R10 addresses, which select the main 4Meg sub-arrays, need to be the LSBs in the counting scheme. Therefore, that is the default condition. Attached tables (see sheet "COUNTING") have the counting details. TM-F-2, TM-F-3

15	(open)	No mode assigned to this bit.
16	TMRDOFF	This mode disables the redundancy. It is of course most useful for post-packaging when the need to go back and see what was repaired is needed. DO NOT USE TMRDOFF <16> and TMRDEN <10> at the same time.
17	TMWLS	This is the multi-wordline select mode. With each ACT (or REF) command, more wordlines are activated, and added to the previous ones which remain in a active state. Precharging the banks will cancel all the wordlines. NOTE - VPP should be forced for this test, and the activation rate should be kept low to limit the power (ACT-ACT=100nS??). The activation scheme "remembers" the row pre-decode combinations ie. Once RP987<3> has been selected, it will remain active until precharge. These are the groupings for predecode: 987, 654,32,10 The banks, and R11/R10 are of course not grouped. There are basically two ways to select the wordlines. 1) Using ACT commands and providing a key sequence of row addresses which access all the predecode combinations the fastest. TMRPAD must not be used for this method since the tester must have complete control over the address inputs. The attached table (see sheet "TMWLS") shows an example of how to select all the rows the quickest using this method. Table TM-C-1 32 cycles would be needed for all the normal wordlines. An additional 8 cycles would be needed to include the spares. 2) Using either TMRPAD/ACT commands or REF commands, both of which use the chip's row counters. These counters will automatically select the best sequence for selecting wordlines if in TMWLS mode. Basically the 6,5,4 and 3 addresses count in parallel with the 9,8,7 addresses. Typically 4096 cycles are needed to select all of the row addresses. (this assumes the TM4BK method is used so all banks operate in parallel.) R<11:0> = 12 row address, 2^12=4096 In this mode, only 256 cycles are needed. R<11,10,9:7,2:0>=8 Row addresses, 2^8=256 If the TMRDEN=1 mode is active (spare testing), an additional 32 cycles are needed to select all the wordlines. ***** Obviously method #1 (ACT cycles with no TMRPAD) is faster, but it probably won't be used. The counting scheme in method #2 (REF or TMRPAD/ACT) was chosen so it is the most compatible with the TMWLTB mode (tm#26) as well. Consideration was given to functional testing, not just bringing wordlines up as quick as possible for DC stressing. Summary: Stress all rows, no spares: 256 cycles Stress all rows, with spares: 288 cycles Stress half rows, no spares: 128 cycles (TMA0<0 or 1> active) Stress half rows, with spares: 144 cycles (TMA0<0 or 1> active) Several other test modes should be used with this: a) Turn off VPP via the VSR register and force directly. b) Turn off VBLEQ via the VSR register and set (or force) VBLEQ=0V c) use TM#27, TMSAOFB, to disable any sensing. d) TM4BK should be used for the best efficiency (don't care if REF method used). e) TMA0<0:1> can be used to select even or odd wordlines (TMRPAD or REF only).

18 TMFSEN This is the "fast" sensing mode. The dummy wordline timer is sped up so the ln/lp signals will fire about 1.4ns faster. This is probably not useful fo a production basis, but will help in analyzing the part.
See the ROW1K/DWLGEN schematic for details.

19 TMSSEN This is the "slow" sensing mode. The SEN signal is slowed down by about 1ns. It may be useful for detecting weak columns in a minimum TRCD situation. It will certainly be useful for analyzing the design.
See the ROW1K/SENSH schematic for details.

20 TMEISO This selects the "early ISO" method of sensing. The ISO signal for a selected sub-array goes high immediately, not some delay after sensing has started.
This mode could help restore time, it could hurt min TRCD values.
Its purpose is mostly for design analysis.
See ROW1K/ISOEN schematic for details.

21 TMOUT This mode puts various signals out through 3 of the DQ buffers.
This is also the mode from which to read the chip ID fuses.
When activated, all the normal output buffers and paths are deactivated.
Only the DQs listed below are on, and they put out the signals as indicated.

DQ<2> = n/a
DQ<6> = Fuse ID information
DQ<9> = QCLK (DLL output)
DQ<13> = REGPLSB (oscillator output)

Further notes on reading the chip ID fuses.
After entering the TMOUT mode, the fuses must be set. This requires a BST command with A<10>="1"

To increment to the next fuse, issue a BST command with A<10>="0".
Each BST command only puts out the next fuse (+1), there is no DDR type function of this mode.
There are a total of 80 fuses, so 79 increments will be required to read them all.
(see TMBLK/TKFS schematic for details)

22 TMCOMP This is the x4 compression test mode. Only DQs 2,6,9, and 13 are active.
8 bits are actually read out as this mode works in DDR.
All the write data is derived from the XY scramble register. The read data is simply pass (="1") and fail (="0").
The column address field is X16 (no C11 or C9), so 32 bits are written and compared internally. Each bit is compared individually with its expected answer so there is no chance of a "false pass". If any bit within a group of 4 fails, a fail (=0) is registered for that master bit. The 4-bit groups are organized such that any fail bit requires replacing all four bits for the repair anyway.

DQ<2> = internal 0,1,2,3
DQ<6> = internal 4,5,6,7
DQ<9> = internal 11,10,9,8
DQ<13> = internal 15,14,13,12

The four DQs chosen for compression are of course the same as for X4 mode.
They correspond to the C119<2> address.
The odd and even parts of the data written from the XY scramble register will always be the same. Even in TMRPAD mode, the A<0> pad for columns (C0) can be modulated to determine which data you would like to read first, however, we recommend just leaving C0=0.

TMSCLK <9> must also be used since the write data path is slower, also maximum frequency of operation is limited due to the slower read path (<125Mhz?).
NOTE - in TMRPAD mode, you must use TMCOMP !!

23	TMX1	This is the x1 compression test mode. TMCOMP must also be set for this to work. DQ<6> is the single active output, it of course just reads pass/fail information Rising and falling data are also combined, so only the rising edge need be strobed. Since repair analysis can't be done, this is most useful in a burn-in or other package situations.
24	(open)	No mode assigned to this bit.
25	TMRPAD	This is the reduced pad test mode. See section (F) for complete details since this section is so lengthy.
26	TMWLTB	This is the wordline toggle mode. It is a VPP level signal, active low. (Still set the bit="1" to activate) In this mode every previous row selected is "remembered" and selected again. Thus, the first active cycle would bring up 1 wordline, the next 2, the next 3, and so forth. It can be combined with the TMWLS mode and be really effective in toggling a lot of wordlines at once. (Only one of the 4 PHIX signals is toggled per cycle. Although the previous row addresses may be "remembered", they will only toggle if their PHIX address is a match on that cycle.) CAUTION - this mode will consume a lot of power. Trc_min=??ns at this time. We are not sure this mode will be needed, but it is available. In TMRPAD, this is the best sequence we found using simulations. (REF can't be used for the selection process since it always INCs.) (see section (F), TMRPAD, for detailed definition of these commands) a)Load the background data b) set TMWLS, TMWLTB, TM4BK, TM11MS, and either TMA0<0 or 1> c) Do 7 ACTs with XINC, and a 8th ACT with no INC. (This will activate 32 wordlines in four banks) d) Do a PRE command and set the TMXREV mode (A0=1). e) Do several ACT/PRE commands with no INC. The wordlines active on the last PHIX selected are being toggled. f) On the last ACT, use the INC to 'back up one". g) Repeat the ACT/PRE sequences on the other PHIX wordlines. (The remaining two PHIXs are not being selected, this is a odd or even test only.) h) When enough cycles have been completed, move the counter forward 2 cycles and select the next group of 8 wordlines. I) How many cycles are done before refreshing and/or reading the stored data will be a function of the actual test. REMEMBER- This is a very power intensive test since the wordlines are being toggled, not just selected and kept high. This limits the number of rows that can be selected before proceeding with the toggling stress. Although simulations have been run to verify this mode, we will run tests on actual wafers and update this test method accordingly.
27	TMSAOFB	This is the disable sensing mode. It is a VPP level signal, active low. (Still set the bit="1" to activate) This mode only disables the sensing, keeping the array sense-amps in a "precharge" state. Combined with forcing VBLEQ=0V, this mode will most likely be used during various wafer level stress tests.

D) Detailed description of Voltage Set Registers

Section B describes how to load the VOLTAGE SET REGISTER (VSR).
The sheet "REGISTER" shows an example of the 8x4 VSR.

Each generated supply on the chip can be modulated via a test mode.
They can also be modulated via fuses.
(There are no fuses for VBLEQ,VPL, and VRAT)

If a test mode is invoked, it supercedes the fuse information.
This means the fuses can be totally ignored and the voltage will be determined by the equation in the VSR register.

Any time the contents of the VSR register="0000" for a particular supply, the value is determined by the fuses.

Two key sheets are attached, "SOFT SET INFO" and "FUSE BLOW INFO".
table TM-D-1 table TM-D-2

They indicate in detail how to modulate each supply.
Note, the "fuse" information is provided from a slightly different perspective.
Given a value measured at pre-fuse, the "FUSE BLOW INFO" table explains which fuses to blow in order to reach the intended target.

When measuring values of pumped supplies at pre-fuse (VPP,VNWL,VBB), the RATIO (VRAT) mode should be used to set VINT at 2.0V and VBLH at 1.6V.
(Unless the VRAT register is changed, a VCCX=2.5V will provide these target values of VINT=2.0 and VBLH=1.6V.)

In RATIO mode the bandgap is bypassed and the Vbg_ref voltage is derived as a function of VCCX. VINT and VBLH then are also straight ratios of VCCX, as defined in the table.
Generally though, VPP, VNWL, and VBB should not be measured with the intent of trimming fuses. The fuses are mainly provided to accommodate future changes in the target voltages. This will reduce the need for mask changes.
If VPP, VNWL, or VBB are not at their target voltages (given VINT and VBLH are correct), then a defect is present and trimming fuses will not solve the issue.

VBB ** **NOTE- The current default value of the design is VBB=-0.3V.**
The current production target is VBB=0V, so fuses will have to be blown on each die to achieve this. 12/26/01

The "SOFT SET INFO" mostly pertains to modulating the voltages after fuse blow. However, some of the functions are most useful at pre-fuse.
For example, during TMWLS wordline stressing, the VPP generator should be turned off (code="0111").

VREF is internally generated for SDR parts and while in TMRPAD mode.
The generation of VREF is a strict ratio of VINT.
The VREF register bits can modulate this ratio.

There are no fuses for the VPL/VBLEQ control. Just soft set control to aid in the finding of weak bits and characterization.

E) Detailed description of XY Scramble Control Register

(see table TM-D-2, sheet "registers" if .xls file is open)

The XY scramble register controls the data pattern that is used in TMCOMP mode. In TMCOMP, no data is written to the chip from external sources, it is all derived from the XY scramble register. For reading, the data from the array is compared with the expected result from the XY register and determined to be pass or fail.

The XY register is set up to mimic a 4row x 8bitline matrix of memory cells. The 8 bitlines are basically two groups of 4, each group of 4 corresponds to a Y-select address. Thus the top half of the matrix is matched with C1=0, the bottom half with C1=1.
The 4 bits within a column group would always be accessed and repaired together. (For normal mode X4 and X8 parts, the C<11,9> addresses are used to select individual portions of this 4 bit group.)

The actual XY register is 4x4 bits.
The XY<0> line denotes the pattern to be used for the Read Row scramble.
The XY<1> line denotes the pattern to be used for the Write Row scramble.
The row pattern can be different for reading and writing to facilitate RMW patterns.
The XY<2> register line corresponds to the 4 bitlines for C1<0>.
The XY<3> line corresponds to the 4 bitlines for C1<1>. {C1 is the A<1> column address.}

For any given cycle, the data is generated by an EXOR of the correct row and bitline information.
First, a determination is made on reading (use the XR line) or writing (use the XW line).
Then, the last two bits of the row address(X<1:0>) are used to determine which of the 4 rows is active. One register bit is now selected to correspond with the row information.
The C1 address is compared in order to see which 4 bits to use for the the bitline information. This would be the same for reading and writing.
4 data bits are then generated (TKD<0:3>), by EXORing each bitline bit with the selected row bit.

If the answer to the EXOR equation is a "1", then an internal "1" will be written to that cell location. Opposite for a "0".

The data can of course be inverted by use of the TMINV mode (defined in section (F)).

{ The correct internal data is achieved by passing the desired information through a set of logic that implements the chip's data scramble. The tester would normally do this function, but that is not compatible with this type of compression.
The user does not need any knowledge of this scramble.
Just program the desired cell states into the XY register, and the chip's logic will generate the correct data scramble to make sure it is correct. }

Some further notes on the scramble:
The same data is written to all the even and odd I/Os.

I/O <0> maps to <0,4,11,15> identically,	maps to TKD<0>
I/O <1> maps to <1,5,10,14> identically,	maps to TKD<1>
I/O <2> maps to <2,6,9,13> identically,	maps to TKD<2>
I/O <3> maps to <3,7,8,12> identically,	maps to TKD<3>

The scramble was changed from the S17 version, so the bank address is not involved. This allows easy implementation of the TM4BK mode.
The same data can be written to all four banks in parallel and be topologically correct.

Remember, the 4x8 matrix is of memory cell trench positions, not row addresses. The upper left most cell is actually accessed by wordline <1> (X1=0, X0=1).
Wordline <0> (X1=0,X0=0) actually accesses the second trench over to the right.

This 4x8 matrix of cells is set-up to mimic the top left sub-array in the chip. (Bank<0>, R11<0>, R10<0>.
In the case that R10<1> is valid, the physical position of I/O <0> and <2> swap.
I/Os <1> and <3> also swap.
The XY register definitions do not comprehend this, but of course the scramble equations do. As long as two pass testing is done (data then data-bar), this change in the mapping can be ignored.
example: A column stripe pattern is desired for a particular row.
I/Os <0,2,1,3> are programmed as <"1","0","1","0"> for the C1<0> line in XY Reg.
I/Os <1,3,0,2> are programmed as <"1","0","1","0"> for the C1<1> line in XY Reg.
For the R10<0> sub-arrays, this will be the result along a row, 10101010 etc.
However, in the R10<1> sub-arrays, the result will be 01010101 etc.
As you can see, in the next pass when the data is inverted, the opposite case will be covered.
Of course, the XY register can always be reprogrammed to comprehend this I/O swapping in the R10<1> cases.

F) Detailed description of TMRPAD mode.

There are two ways to enter.

1) By IO configuration X16VCC=0 DQ8=0 DQ7=0

2) By accessing the TMRPAD bit in the main test register.

TMCOMP <22> and TMSCLK <9> must also be selected for functional results.

Normal MRS and EMRS Register loads are invalid in TMRPAD.
The configuration will be DDR, CL<2>, BL<2>, SEQ, DLL-OFF, Full Strength I/O

These pads must be probed and hooked to active tester channels.

CLK
WE/CAS/RAS for control
A<11,10,7,0> not for addressing, but for loading the test mode register and generating special TMRPAD commands.
(A<0> is active as such for columns.)

DQ<2,6,9,13> for reading only, DDR outputs.
UDM, only for measuring voltages per TMOUT mode, no masking allowed.

Required probe, optional tester channel
CSB this pad needs to be held at VSS (always active), or it could be hooked to a active CSB tester channel if desired.

X16VCC, DQ<8>, DQ<7> for wafer probe, these need to be 0V so TMRPAD can be entered.

These pins required to be HI-Z, or not probed
VREF this is generated internally, any probing could conflict with the result.
CLKB this is internally shorted to VREF, any probing could conflict.

These pins can be floated or grounded (TMRPAD will ground them anyway)
BA<1,0>
A<9,8,6,5,4,3,2,1>
DQ<15,14,12,11,10,5,4,3,1,0>
LDM
DDRPAD
DQS<0,1>

These pins can be measured or forced if desired
VINT
VBLH
VNWL
VBB
VPP

At least one of each of these supplies is needed. VCCX can equal VCCQ.
VCCX
VCCQ
VSS
VSSQ

Extended Commands / Modes

Since all row and column address are generated by the chip, and the tester must track these addresses for repair purposes, several extra functions are added in TMRPAD mode to facilitate this.
In general, for a given command, the state of addresses 11,10,7, and 0 are sampled to see if any extra commands should be executed.

INCREMENTING THE ROW COUNTERS

ACTIVE

11	10	7	0	
1	x	x	x	increment bank row address
x	1	x	x	increment row address

The internal increment is after the ACT command, so the NEXT address will be seen as ROW+1 or BANK+1.
ROW_BANK INC and ROW INC can be combined in same cycle.
A<7,0> not used for ACT cycles.
(Refer to the TMBLK/TKACT schematic for details)

INCREMENTING THE COL COUNTERS

READ/WRITE

11	10	7	0	
1	x	x	x	increment bank col address
x	x	1	x	increment col address

The internal increment is after the READ/WRITE command, so the NEXT address will be seen as COL+1 or BANK+1.
COL_BANK INC and COL INC can be combined in same cycle.
A<0> is still used as the start address for DDR out in TMRPAD.
A<10> is still used as the Auto-Precharge indicator in TMRPAD.
(Refer to the TMBLK/TKYINCB schematic for details)

RESETTING THE COUNTERS

BST

11	10	7	0	
1	x	x	x	reset bank column counters=00
x	1	x	x	reset row (and bank row) address
x	x	1	x	reset col address

A<0> not used for BST cycles.
All three resets can be combined or grouped on a single command.
The bank column always resets to bank=0.
The bank row always resets to bank=0.
(Refer to the TMBLK/TKRES schematic for details)

The row address resets as follows: Xspare - X Start Address

TMXREV	TMRDEN	X<99> - X<11:0> hex
0	0	0-000
0	1	0-000
1	0	0-FFF
1	1	1-C07

X<99> is the spare row address.
Refer to counting tables TM-F-1,2,3,4 for complete details on row counting in TMRDEN and reverse mode. (see sheet "count" in .xls file)

The col address resets as follows: Yspare - Y Start Address

TMYREV	TMRDEN	Y<99> - Y<8:0> hex
0	0	0-000
0	1	0-000
1	0	0-1FE
1	1	1-10C

A<0> does not have a column counter bit, equal to the pad.
Y<99> is the spare row address.
Refer to counting tables TM-F-1,2 for complete details on column counting in TMRDEN and reverse mode. (see sheet "count" in .xls file)

TMINV
TMXREV
TMYREV

REVERSING THE COUNTERS / INVERTING the DATA

PRECHARGE	11	10	7	0	
	0/1	1	x	x	1=invert data from TDATA generator (TMINV=1)
	x	1	0/ 1	x	1=reverse count mode for Y-address, (TMYREV=1)
	x	1	x	0/1	1=reverse count mode for X-address, (TMXREV=1)

These commands are only valid for a PRE-ALL command (A<10>="1")
Any combination of this table can be used in the same command.

The reverse mode and data inversion commands are not part of the general test mode register so that they can be modified during an actual test pattern.
Example, the test register could be programmed for a certain row march pattern. Then upon completion of the first pass, the data could be inverted for the entire second pass without reprogramming all the registers.

The reverse mode can be utilized to "back-up" while in a pattern. This is especially usefull when combining the TMWLS and TMWLTB modes.

In general it is our intention that the reverse modes never be used. Reads with "positive write back", instead of R-M-W cycles should be used in any pattern previously requiring reverse counting.
(see TMBLK/TMINVREV schematic for details)

There is NO reverse counting for the bank row or column counters.
Bank resets always return to Bank<0>, the count order is <0,1,2,3,0,1…>

MAIN TEST REGISTER (MTR) TM-B-1

	<11>		<10>		<7>		<0>	
0	VMEAS <3>	3	VMEAS <2>	2	VMEAS <1>	1	VMEAS	0
1	CBRUP	7	CBRSHT	6	RAS	5	4BK	4
2		11	RDEN	10	SCLK	9	CKE0	8
3		15	R11MS	14	A0<0>	13	A0<1>	12
4	SSEN	19	FSEN	18	WLS	17	RDOFF	16
5	X1	23	COMP	22	OUT	21	EISO	20
6	SAOFB	27	WLTB	26	RPAD	25		24

**DON'T ACTIVATE 12,13 AT SAME TIME

**DON'T ACTIVATE 10,16 AT SAME TIME

TMRPAD IS ALSO GENERATED BY X16PAD=DQ<8>=DQ<7>=0V FOR WAFER PROBE.

TMSAOFB IS THE INVERSE Vpp LEVEL OF TM<27>

TM<22> NEEDS TO BE SET IN REDPAD MODE

TM<7,22> PROBABLY NEED TM<9> SET TOO

TMWLTB IS THE INVERSE Vpp LEVEL OF TM<26>

TM <8> ONLY VALID IN RPAD MODE

XY SCRAMBLE TEST REGISTER (XY) TM-B-2

	<11>	<10>	<7>	<0>	
0	X1,0<1>	X1,0<0>	X1,0<3>	X1,0<2>	X- READ CONFIGURE
1	X1,0<1>	X1,0<0>	X1,0<3>	X1,0<2>	X- WRITE CONFIGURE
2	I/O<0>	I/O<2>	I/O<1>	I/O<3>	Y C1=0 CONFIGURE
3	I/O<1>	I/O<3>	I/O<0>	I/O<2>	Y C1=1 CONFIGURE

CELL Matrix Diagram

		A<11>	A<10>	A<7>	A<0> << XY Register Program ˅ ˅	
Wordline (X1,0)>>		<1>	<0>	<3>	<2>	
X0	>>	1	0	1	0	
X1	>>	0	0	1	1	
C1<0>	I/O <0>	**O**	**O**	**O**	**O**	A<11>
	I/O <2>	**O**	**O**	**O**	**O**	A<10>
	I/O <1>	**O**	**O**	**O**	**O**	A<7>
	I/O <3>	**O**	**O**	**O**	**O**	A<0>
C1<1>	I/O <1>	**O**	**O**	**O**	**O**	A<11>
	I/O <3>	**O**	**O**	**O**	**O**	A<10>
	I/O <0>	**O**	**O**	**O**	**O**	A<7>
	I/O <2>	**O**	**O**	**O**	**O**	A<0>

O=TRENCH POSITION

Data for each I/O is an EXOR of the row register bit (read or write), and the correct C1 address<0 or 1>.

**REPEATS for groups of 4 wordlines to the right, cell matrix only checks X1 and X0.
**REPEATS for groups of 8 bitlines to the bottom, cell matrix only checks C1.

**I/Os <0> and <2> swap physical position for sub-arrays with R10<1>.
**I/Os <1> and <3> swap physical position for sub-arrays with R10<1>.
See Section (E) in DESC for complete details.

(VSR) TM-B-3

VOLTAGE SET TEST REGISTER

	<11>	<10>	<7>	<0>	
0					VINT
1					VBLH
2					VPP
3					VPL
4					VBLEQ
5	REF	REF	RAT	RAT	REF/RAT
6					VBB
7					VNWL

See Sheet "SOFT SET INFO" for details on how the individual bits program each supply (table TM-D-1).

table TM-D-1

SOFT SET INFORMATION FOR GENERATED VOLTAGES

VINT

ADDRESS				VINT@ VBG=1.25
11	10	7	0	
0	0	0	0	READ FUSES
0	0	0	1	1.951
0	0	1	0	1.905
0	0	1	1	1.860
0	1	0	0	1.818
0	1	0	1	1.778
0	1	1	0	1.739
0	1	1	1	1.702
1	0	0	0	2.000
1	0	0	1	2.424
1	0	1	0	2.353
1	0	1	1	2.286
1	1	0	0	2.222
1	1	0	1	2.162
1	1	1	0	2.105
1	1	1	1	VINT=VEXT

Default design:
VINT=1.6*VBG

VBLH

ADDRESS				VBLH@ VBG=1.25
11	10	7	0	
0	0	0	0	READ FUSES
0	0	0	1	1.56
0	0	1	0	1.52
0	0	1	1	1.49
0	1	0	0	1.45
0	1	0	1	1.42
0	1	1	0	1.39
0	1	1	1	1.36
1	0	0	0	1.60
1	0	0	1	1.94
1	0	1	0	1.88
1	0	1	1	1.83
1	1	0	0	1.78
1	1	0	1	1.73
1	1	1	0	1.68
1	1	1	1	VBLH=VEXT

Default design:
VBLH=1.28*VBG

VPL

ADDRESS				VPL VALUE FOR VBLH=1.6V
11	10	7	0	
0	0	0	0	0.8
0	0	0	1	VSS
0	0	1	0	0.525
0	0	1	1	0.575
0	1	0	0	0.625
0	1	0	1	0.675
0	1	1	0	0.725
0	1	1	1	0.775
1	0	0	0	0.825
1	0	0	1	0.875
1	0	1	0	0.925
1	0	1	1	0.975
1	1	0	0	1.025
1	1	0	1	1.075
1	1	1	0	VBLH
1	1	1	1	TRISTATE

Default design:
VPL=0.5*VBLH

VPP

ADDRESS				VPP VALUE FOR VBLH=1.6V
11	10	7	0	
0	0	0	0	READ FUSES
0	0	0	1	3.00
0	0	1	0	3.10
0	0	1	1	3.20
0	1	0	0	3.30
0	1	0	1	3.40
0	1	1	0	PUMP ON
0	1	1	1	PUMP OFF
1	0	0	0	2.90
1	0	0	1	2.20
1	0	1	0	2.30
1	0	1	1	2.40
1	1	0	0	2.50
1	1	0	1	2.60
1	1	1	0	2.70
1	1	1	1	2.80

Default design:
VPP=1.81*VBLH

VBB

ADDRESS				VBB VALUE FOR VINT=2V
11	10	7	0	
0	0	0	0	READ FUSES
0	0	0	1	-0.22
0	0	1	0	-0.15
0	0	1	1	-0.09
0	1	0	0	-0.30
0	1	0	1	VBB=VSS
0	1	1	0	PUMP OFF
0	1	1	1	PUMP ON
1	0	0	0	-1.70*
1	0	0	1	-1.38*
1	0	1	0	-1.13*
1	0	1	1	-0.92
1	1	0	0	-0.75
1	1	0	1	-0.61
1	1	1	0	-0.49
1	1	1	1	-0.39

Default design:
VBB= -0.15*VINT

VNWLL

ADDRESS				VNWLL VALUE FOR VINT=2V
11	10	7	0	
0	0	0	0	READ FUSES
0	0	0	1	(0.11x) -.22V
0	0	1	0	-0.15
0	0	1	1	-0.09
0	1	0	0	-0.30
0	1	0	1	VNWL=VSS
0	1	1	0	PUMP OFF
0	1	1	1	PUMP ON
1	0	0	0	-1.70*
1	0	0	1	-1.38*
1	0	1	0	-1.13*
1	0	1	1	-0.92
1	1	0	0	-0.75
1	1	0	1	-0.61
1	1	1	0	-0.49
1	1	1	1	-0.39

Default design:
VNWL= -0.15*VINT

(use 0.11x for burn-in,
0.11x2.8V=0.31V)

VBLEQ

ADDRESS				VBLEQ VALUE FOR VBLH=1.6V
11	10	7	0	
0	0	0	0	0.8
0	0	0	1	VSS
0	0	1	0	0.525
0	0	1	1	0.575
0	1	0	0	0.625
0	1	0	1	0.675
0	1	1	0	0.725
0	1	1	1	0.775
1	0	0	0	0.825
1	0	0	1	0.875
1	0	1	0	0.925
1	0	1	1	0.975
1	1	0	0	1.025
1	1	0	1	1.075
1	1	1	0	VBLH
1	1	1	1	TRISTATE

Default design:
VBLEQ=0.5*VBLH

VREF (input reference)

ADDRESS				VREF VREF:VINT RATIO
11	10			SDR /LPSDR
0	0	X	X	READ FUSES
0	1	X	X	0.6 / 0.485
1	0	X	X	0.75 / 0.675
1	1	X	X	0.7 / 0.61

Default design:
VREF=0.65*VINT
(.55 for LPSDR)

TMRPAD uses SDR (LPSDR different than SDR since vih/vil specs are lower)

VRAT

				VRAT VINT/VCCX RATIO	VRAT VBLH/VCCX RATIO
		7	0		
X	X	0	0	VBG USED	VBG USED
X	X	0	1	0.80	0.64
X	X	1	0	1.00	0.80
X	X	1	1	0.92	0.74

Default design: VBG=1.25V

VREF and VRAT entered in same VSR register,
Bits<11,10 are for VREF, <7,0> for VRAT

* VBB and VNWLL pumps will only pump to about -1.1V, unloaded.

See section (b), (sheet "Registers"), for how to load these registers.

** Pump-on means the pump runs at full speed with no regulation.
This is the easiest way to determine the pump's highest output capability.

"Tri-state" and "pump-off" mean that generator is disabled and the voltage must be forced by the tester.

Voltage Generation Tree

VBG or VRAT determine VINT and VBLH values.
VINT determines VNWL,VBB and VREF values.
VBLH determines VPP, VPL, and VBLEQ values.

table TM-D-2

FUSE BLOW INFORMATION FOR GENERATED VOLTAGES

VINT

FUSE TO BE BLOWN				MEASURED PREFUSE VINT
F3	F2	F1	F0	
				2
			X	2.05
		X		2.10
		X	X	2.15
	X			2.20
	X		X	2.25
	X	X		2.30
	X	X	X	2.35
X				2.00
X			X	1.65
X		X		1.70
X		X	X	1.75
X	X			1.80
X	X		X	1.85
X	X	X		1.90
X	X	X	X	NOTE 1

VBLH

FUSE TO BE BLOWN				MEASURED PREFUSE VBLH
F3	F2	F1	F0	
				1.6
			X	1.64
		X		1.68
		X	X	1.72
	X			1.76
	X		X	1.80
	X	X		1.84
	X	X	X	1.88
X				1.60
X			X	1.32
X		X		1.36
X		X	X	1.40
X	X			1.44
X	X		X	1.48
X	X	X		1.52
X	X	X	X	NOTE 1

VPP

FUSE TO BE BLOWN				VPP VALUE FOR VBLH=1.6V
F3	F2	F1	F0	
				2.90
			X	3.00
		X		3.10
		X	X	3.20
	X			3.30
	X		X	3.40
	X	X		PUMP ON
	X	X	X	PUMP OFF
X				2.90
X			X	2.20
X		X		2.30
X		X	X	2.40
X	X			2.50
X	X		X	2.60
X	X	X		2.70
X	X	X	X	2.80

VBB

FUSE TO BE BLOWN				VBB VALUE FOR VINT=2V
F3	F2	F1	F0	
				-0.30
			X	-0.22
		X		-0.15
		X	X	-0.09
	X			-0.30
	X		X	VBB=VSS
	X	X		PUMP OFF
	X	X	X	PUMP ON
X				-1.70*
X			X	-1.38*
X		X		-1.13*
X		X	X	-0.92
X	X			-0.75
X	X		X	-0.61
X	X	X		-0.49
X	X	X	X	-0.39

VNWLL

FUSE TO BE BLOWN				VNWLL VALUE FOR VINT=2V
F3	F2	F1	F0	
				-0.30
			X	-0.22
		X		-0.15
		X	X	-0.09
	X			-0.30
	X		X	VNWL=VSS
	X	X		PUMP OFF
	X	X	X	PUMP ON
X				-1.70*
X			X	-1.38*
X		X		-1.13*
X		X	X	-0.92
X	X			-0.75
X	X		X	-0.61
X	X	X		-0.49
X	X	X	X	-0.39

VREF

FUSE TO BE BLOWN				VREF VREF:VINT RATIO
F3	F2	F1	F0	SDR/LPSDR
				0.65/0.55
	X			0.6/0.485
X				0.75/0.675
X	X			0.7/0.61

NOTE 1: If all fuses are blown, VINT or VBLH will be shorted to VEXT.
* VBB and VNWLL pumps will only pump to about -1.1V, unloaded.
See Fuse Location Table for X,Y fuse coordinates.

12/20/2001

This table is only valid for the target values as indicated.
Should the target change (example VINT target=2.05V),
then this table does not apply and the values should be derived from table TM-D-1.

XCOUNT

Table TM-F-1 Row Counting

Normal Mode: (no test modes active), this is the normal REF command count sequence, forward only.

Test Modes:

TMRPAD=0 or 1 (If TMRPAD=0, this only applies to REF cycles)
TMRDEN=0
TMR11MS=0
TMXREV=0 or 1

	MSB											LSB	
A>> <99>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	<11>	<10>	R<11:10> define sub-array
						etc.							
0	1	1	1	1	1	1	1	1	1	1	0	0	
0	1	1	1	1	1	1	1	1	1	1	0	1	
0	1	1	1	1	1	1	1	1	1	1	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	<< Reset here if TMXREV=1
0	0	0	0	0	0	0	0	0	0	0	0	0	<< Reset here if TMXREV=0
0	0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	0	
0	0	0	0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0	0	0	1	0	0	
0	0	0	0	0	0	0	0	0	0	1	0	1	
						etc.							
	v									^			
	v	Direction for forward count (TMXREV=0)								^	Direction for reverse count (TMXREV=1)		

<99>=spare

Table TM-F-2 Row Counting

Test Modes:

TMRPAD=0 or 1 (If TMRPAD=0, this only applies to REF cycles)
TMRDEN=0
TMR11MS=1
TMXREV=0 or 1

A>>	<99>	MSB <11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	LSB <0>	R<11:10> define sub-array
							etc.							
0	1	1	1	1	1	1	1	1	1	1	0	0		
0	1	1	1	1	1	1	1	1	1	1	0	1		
0	1	1	1	1	1	1	1	1	1	1	1	0		
0	1	1	1	1	1	1	1	1	1	1	1	1	<< Reset here if TMXREV=1	
0	0	0	0	0	0	0	0	0	0	0	0	0	<< Reset here if TMXREV=0	
0	0	0	0	0	0	0	0	0	0	0	0	1		
0	0	0	0	0	0	0	0	0	0	0	1	0		
0	0	0	0	0	0	0	0	0	0	0	1	1		
0	0	0	0	0	0	0	0	0	0	1	0	0		
0	0	0	0	0	0	0	0	0	0	1	0	1		
							etc.							

v ^

v Direction for forward count (TMXREV=0) ^ Direction for reverse count (TMXREV=1)

<99>=spare

Table TM-F-3 Row Counting

Test Modes:

TMRPAD=0 or 1 (If TMRPAD=0, this only applies to REF cycles)
TMRDEN=1
TMR11MS=1
TMXREV=0 or 1

MSB A>> <99>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	LSB <0>	R<11:10> define sub-array
						etc.							
0	1	1	1	1	1	1	1	1	1	1	0	0	
0	1	1	1	1	1	1	1	1	1	1	0	1	
0	1	1	1	1	1	1	1	1	1	1	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	(last real row)
1	0	0	0	0	0	0	0	0	0	0	0	0	(SP0,1st sub-array)
1	0	0	0	0	0	0	0	0	0	0	0	1	(SP1)
1	0	0	0	0	0	0	0	0	0	0	1	0	(SP2)
1	0	0	0	0	0	0	0	0	0	0	1	1	(SP3)
1	0	0	0	0	0	0	0	0	0	1	0	0	(SP4)
1	0	0	0	0	0	0	0	0	0	1	0	1	(SP5)
1	0	0	0	0	0	0	0	0	0	1	1	0	(SP6)
1	0	0	0	0	0	0	0	0	0	1	1	1	(SP7)
1	0	1	0	0	0	0	0	0	0	0	0	0	(SP0, 2nd sub-array)
					etc.								
			Only 11,10,2,1,0 count in this region (9:3="0")										
1	1	1	0	0	0	0	0	0	0	1	1	0	(SP6, 4th sub-array)
1	1	1	0	0	0	0	0	0	0	1	1	1	<< Reset here if TMXREV=1
0	0	0	0	0	0	0	0	0	0	0	0	0	<< Reset here if TMXREV=0
0	0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	0	
0	0	0	0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0	0	0	1	0	0	
0	0	0	0	0	0	0	0	0	0	1	0	1	
						etc.							

v ^

v Direction for forward count (TMXREV=0) ^ Direction for reverse count (TMXREV=1)

<99>=spare

Table TM-F-4 Row Counting

Test Modes:

TMRPAD=0 or 1 (If TMRPAD=0, this only applies to REF cycles)
TMRDEN=1
TMR11MS=0
TMXREV=0 or 1

MSB A>> <99>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	<11>	LSB <10>	R<11:10> define sub-array
						etc.							
0	1	1	1	1	1	1	1	1	1	1	0	0	
0	1	1	1	1	1	1	1	1	1	1	0	1	
0	1	1	1	1	1	1	1	1	1	1	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	(last real row)
1	0	0	0	0	0	0	0	0	0	0	0	0	(SP0, 1st sub-array)
1	0	0	0	0	0	0	0	0	0	0	0	1	(SP0, 2nd sub-array)
1	0	0	0	0	0	0	0	0	0	0	1	0	(SP0, 3rd sub-array)
1	0	0	0	0	0	0	0	0	0	0	1	1	(SP0, 4th sub-array)
1	0	0	0	0	0	0	0	0	0	1	0	0	(SP1, first sub-array)
1	0	0	0	0	0	0	0	0	0	1	0	1	(SP1, 2nd sub-array)
1	0	0	0	0	0	0	0	0	0	1	1	0	(SP1, 3rd sub-array)
1	0	0	0	0	0	0	0	0	0	1	1	1	(SP1, 4th sub-array)
1	0	0	0	0	0	0	0	0	1	0	0	0	
		etc.											
	Only 11,10,2,1,0 count in this region (9:3="0")												
1	0	0	0	0	0	0	0	1	1	1	1	0	(SP7, 3rd sub-array)
1	0	0	0	0	0	0	0	1	1	1	1	1	<< Reset here if TMXREV=1
0	0	0	0	0	0	0	0	0	0	0	0	0	<< Reset here if TMXREV=0
0	0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	0	
0	0	0	0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0	0	0	1	0	0	
0	0	0	0	0	0	0	0	0	0	1	0	1	
						etc.							
	v									^			
	v	Direction for forward count (TMXREV=0)								^	Direction for reverse count (TMXREV=1)		

<99>=spare

YCOUNT

Table TM-F-5 Column Counting

(These column counting schemes only apply to TMRPAD mode.
The burst counting used in normal mode varies by burst length and type.
Those counting methods are well established and defined in the data sheets.)

Test Modes:

TMRPAD=1
TMRDEN=0
TMYREV=0 or 1

A>>	<99>	MSB <8>	<7>	<6>	<5>	<4>	<3>	<2>	LSB <1>	
						etc.				
	0	1	1	1	1	1	1	0	0	
	0	1	1	1	1	1	1	0	1	
	0	1	1	1	1	1	1	1	0	
	0	1	1	1	1	1	1	1	1	<< Reset here if TMYREV=1
	0	0	0	0	0	0	0	0	0	<< Reset here if TMYREV=0
	0	0	0	0	0	0	0	0	1	
	0	0	0	0	0	0	0	1	0	
	0	0	0	0	0	0	0	1	1	
	0	0	0	0	0	0	1	0	0	
	0	0	0	0	0	0	1	0	1	
						etc.				

v ^

v Direction for forward count (TMYREV=0) ^ Direction for reverse count (TMYREV=1)

<99>=spare

C<0> is not part of the counting scheme.
TMRPAD utilizes DDR, so C<0> just defines which
data comes out on rising edge.

Table TM-F-6 Column Counting

(These column counting schemes only apply to TMRPAD mode.
The burst counting used in normal mode varies by burst length and type.
Those counting methods are well established and defined in the data sheets.)

Test Modes:
TMRPAD=1
TMRDEN=1
TMYREV=0 or 1

R<11>	A>>	<99>	MSB <8>	<7>	<6>	<5>	<4>	<3>	<2>	LSB <1>	
							etc.				
x		0	1	1	1	1	1	1	0	0	
x		0	1	1	1	1	1	1	0	1	
x		0	1	1	1	1	1	1	1	0	
x		0	1	1	1	1	1	1	1	1	(last real column)
0/1		1	0	0	0	0	0	0	0	0	(YSP0, C8=0)
0/1		1	0	0	0	0	0	0	1	0	(YSP1, C8=0)
0/1		1	0	0	0	0	0	1	0	0	(YSP2, C8=0)
0/1		1	0	0	0	0	0	1	1	0	(YSP3, C8=0)
0/1		1	1	0	0	0	0	0	0	0	(YSP0, C8=1)
0/1		1	1	0	0	0	0	0	1	0	(YSP1, C8=1)
0/1		1	1	0	0	0	0	1	0	0	(YSP2, C8=1)
0/1		1	1	0	0	0	0	1	1	0	<< Reset here if TMYREV=1
		0	0	0	0	0	0	0	0	0	<< Reset here if TMYREV=0
		0	0	0	0	0	0	0	0	1	
		0	0	0	0	0	0	0	1	0	
		0	0	0	0	0	0	0	1	1	
		0	0	0	0	0	0	1	0	0	
		0	0	0	0	0	0	1	0	1	
					etc.						
	v								^		
	v	Direction for forward count (TMYREV=0)							^	Direction for reverse count (TMYREV=1)	

<99>=spare

C<0> is not part of the counting scheme.
TMRPAD utilizes DDR, so C<0> just defines which
data comes out on rising edge.

C<7,6,5,4,1>="0" For all the spare addresses

Note- As the part is currently configured, the spares are different
for R<11>=0 and R<11>=1. If this scheme is kept intact, it needs to
be accounted for in the testing of the spares.

RECOMMENDED ADDRESS SEQUENCE FOR BRINGING ALL WORDLINES HIGH IN TMWLS,
(Use ACT commands, TMRPAD=0, TM4BK=1)

	BANK (0:3)		4M SUBARY DECODE		987 (0:7)			654 (0:7)			32 (0:3)		PHIX (0:3)		SPARE
ADDRESS	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	LDM
OPEN ALL BANKS (TM4BK=1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	0	0	1	0	0	1	0	1	0	1	0
			0	0	0	1	0	0	1	0	1	0	1	0	0
ACTIVATE ALL WLs IN SUBARRAY 0			0	0	0	1	1	0	1	1	1	1	1	1	0
			0	0	1	0	0	1	0	0					0
			0	0	1	0	1	1	0	1					0
			0	0	1	1	0	1	1	0					0
			0	0	1	1	1	1	1	1					0
			0	1	0	0	0	0	0	0	0	0	0	0	0
			0	1	0	0	1	0	0	1	0	1	0	1	0
			0	1	0	1	0	0	1	0	1	0	1	0	0
ACTIVATE ALL WLs IN SUBARRAY 1			0	1	0	1	1	0	1	1	1	1	1	1	0
			0	1	1	0	0	1	0	0					0
			0	1	1	0	1	1	0	1					0
			0	1	1	1	0	1	1	0					0
			0	1	1	1	1	1	1	1					0
			1	0	0	0	0	0	0	0	0	0	0	0	0
			1	0	0	0	1	0	0	1	0	1	0	1	0
			1	0	0	1	0	0	1	0	1	0	1	0	0
ACTIVATE ALL WLs IN SUBARRAY 2			1	0	0	1	1	0	1	1	1	1	1	1	0
			1	0	1	0	0	1	0	0					0
			1	0	1	0	1	1	0	1					0
			1	0	1	1	0	1	1	0					0
			1	0	1	1	1	1	1	1					0
			1	1	0	0	0	0	0	0	0	0	0	0	0
			1	1	0	0	1	0	0	1	0	1	0	1	0
			1	1	0	1	0	0	1	0	1	0	1	0	0
ACTIVATE ALL WLs IN SUBARRAY 3			1	1	0	1	1	0	1	1	1	1	1	1	0
			1	1	1	0	0	1	0	0					0
			1	1	1	0	1	1	0	1					0
			1	1	1	1	0	1	1	0					0
			1	1	1	1	1	1	1	1					0
ACTIVATE SPARES			0	0	0	0	0	0	0	0	0	0	0	0	1
IN SUBARRAY 0			0	0	0	0	0	0	0	0	0	1			1
ACTIVATE SPARES			0	1	0	0	0	0	0	0	0	0	0	0	1
IN SUBARRAY 1			0	1	0	0	0	0	0	0	0	1			1
ACTIVATE SPARES			1	0	0	0	0	0	0	0	0	0	0	0	1
IN SUBARRAY 2			1	0	0	0	0	0	0	0	0	1			1
ACTIVATE SPARES			1	1	0	0	0	0	0	0	0	0	0	0	1
IN SUBARRAY 3			1	1	0	0	0	0	0	0	0	1			1

NOTES: In TMWLS, once activated, any predecoded signal in that 4M subarray stays high.
VPP power will be high for this sequence; VPP must be forced.
To force odd or even only, keep A0 high or low.
Any addresses not specified are don’t care as those signals are already active.
Spare activation is optional, only if TMRDEN=1

Test Example #1

Attached is an example of the test code needed to load and execute a pattern.
The following items are covered:

i)selecting the test modes based on the test's requirements
ii)selecting the desired cell matrix pattern and correlating it to the XY register.
iii) selecting which voltage supplies that need to be modulated for this particular test and correlating that to loading the VSR register.

iv) After loading the test registers, sample code is presented which indicates how the actual pattern may be run to obtain pass/fail information.

Example Test #1: Basic R-M-W Pattern for Wafer Probe

TMRPAD (wafer probe)
TM4BK and TMR11MS will also be used.
(TMCOMP and TMSCLK must be used since TMRPAD is used)
TMRDEN, Spares are tested (Row and Col)

VINT and VBLH set using the ratio mode to 2.0/1.6V

Row stripe data pattern used
R-M-W, Forward and Backward (Backward use is not recommended, but this
<row fast> is the best example of how it might be used.)

write background, "1"s to even wordlines, "0"s to odd wordlines (>>101010)
read background(>>101010), modify data to inverse
change direction of counters
read inverse data backwards (010101<<), modify data to inverse
read original data(010101<<)backwards,no modify

**Note ** This example does not represent any particular test that may actually be used. It is just an assembly of several different test modes to show by example how they may be used.

1) Set-up

X16VCC,DQ<7,8> should all be forced to 0V so the part is in TMRPAD
VCCX should be set to 2.5V so VINT and VBLH will be correct once VRATIO mode is entered.
The output strobe should be set for CL=2

2) Load the main test mode register, need modes <4,9,10,14,22> active

**intial emrs to enable test mode power can be skipped, because the part is already in TMRPAD by I/O configuration.

	csb/ras/we/cas	<11,10,7,0>	(reference MTR, table TM-B-1
	MRS	1010	Load enable command
	MRS	0011	Select to load Main Test Register
7 load cycles	MRS	0000	load modes <3:0>, none selected
V	MRS	0001	load modes <7:4>, select <4>(TM4BK)
V	MRS	0110	select modes <10,9>,TMRDEN,TMSCLK
	MRS	0100	select mode <14>, TMR11MS
	MRS	0000	load modes <19:16>, none selected
	MRS	0100	select mode <22>, TMCOMP
	MRS	00x0	load modes <27:24>, TMRPAD active by I/O configuration, so bit<25> is don't care.
	NOP		Need non-MRS command to cancel load sequence

3) Load the voltage set register, need VRAT mode

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-3, "registers" sheet
	MRS	1010	Load enable command
	MRS	1011	Select to load Voltage Set Register
8 load cycles	MRS	0000	Vint control, set to default (VRAT will override)
V	MRS	0000	Vblh control, set to default (VRAT will override)
V	MRS	0000	Vpp control, set to default
	MRS	0000	Vpl control, set to default
	MRS	0000	Vbleq control, set to default
	MRS	0001	Vref=default Vrat control, see *** below
	MRS	0000	Vbb control, set to default
	MRS	0000	Vnwl control, set to default
	NOP		Need non-MRS command to cancel load sequence

*** bits <11,10> control VREF, also see table TM-D-1, "soft-set" sheet
VREF will automatically be generated by the chip since TMRPAD is active, it will default to the VREF=0.65*VINT value.

bits <7,0>="0","1" select VINT=.8*VCCX=2.0V (VCCX=2.5V)
VBLH=0.64*VCCX=1.6V

4) Load the XY scramble register, need row stripe pattern
initially set even wordlines (x0=0) to "1"

The following diagram is porvided to help illustrate how the cell matrix
will look with the intended pattern, and how it correlates to loading the register.

X0	>>		1	0	1	0	
X1	>>		0	0	1	1	
C1<0>		I/O <0>	**O**	**I**	**O**	**I**	A<11>
		I/O <2>	**O**	**I**	**O**	**I**	A<10>
		I/O <1>	**O**	**I**	**O**	**I**	A<7>
		I/O <3>	**O**	**I**	**O**	**I**	A<0>
C1<1>		I/O <1>	**O**	**I**	**O**	**I**	A<11>
		I/O <3>	**O**	**I**	**O**	**I**	A<10>
		I/O <0>	**O**	**I**	**O**	**I**	A<7>
		I/O <2>	**O**	**I**	**O**	**I**	A<0>

O=TRENCH POSITION = "0"

I=TRENCH POSITION = "1"

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-2, "registers" sheet
	MRS	1010	Load enable command
	MRS	0111	Select to load XY Register
4 load cycles	MRS	1010	X-read register, load to opposite ****
V	MRS	0101	X-write register, =stripe,even="1"
V	MRS	0000	C1=0 register, no data, set for row stripe
	MRS	0000	C1=1 register, no data, set for row stripe
	NOP		Need non-MRS command to cancel load sequence

**** Loading the Xread register to opposite allows the use of the TMINV (data invert feature. This saves reloading the XY register for a simple change in data state

5) Enable the test modes

csb/ras/we/cas	<11,10,7,0>	
MRS	1111	enable the test modes

At this point all of the registers have been loaded for the initial pass, and the test modes are now active.

6) set the row and col counters to forward direction

	csb/ras/we/cas	<11,10,7,0>	
	PRE-ALL	0100	no data inv, Y=fwd, X=fwd

7) Reset the row and col counters so a known starting point is valid.

	csb/ras/we/cas	<11,10,7,0>	
	BST	111x	bank col, row,col addresses = 00000…

The first pass of the pattern can now be run.

The Xmax address is 1-C07h, and 4096+32=4128 total addresses/bank
The Ymax address is 1-10Ch, and 512+8=520 total addresses/bank
(h=address is in hex)
j-xxx where "j" denotes the spare address

8) Write the background data, row fast, 4 bank parrallel

	csb/ras/we/cas	<11,10,7,0>	
a)	ACT (4)	01xx	inc row address for next active
b)	NOP		(4)=to all four banks in parallel
c)	WRT-A (4)	0100	no increment, auto precharge,even start

<repeat steps (a-c) for all the row addresses>

d)	WRT-A	0110	This is a dummy write, no bank is open, but it will increment the Y-counters. No need to increment the bank column counters since TM4BK is used for writing.

<repeat steps (a-d) for all the column addresses>

9) set the row and col counters to forward direction

	csb/ras/we/cas	<11,10,7,0>	
	PRE-ALL	0100	data inv=yes, Y=fwd, X=fwd
			since the Xread was loaded to be opposite of the Xwrite register, it will now correctly read the previous data, and invert the next write data.

10) Read the background data, row fast, modify the write data

	csb/ras/we/cas	<11,10,7,0>	
a)	ACT (4)	01xx	inc row address for next active
b)	NOP		
c)	READ0-NAP	1000	inc bank col for next read
d)	READ1-NAP	1000	inc bank col for next read
e)	READ2-NAP	1000	inc bank col for next read
f)	READ3-NAP	1000	inc bank col for next read
	NOPS(several)		
g)	WRT-A (4)	0100	no increment, auto precharge,even start

<repeat steps (a-g) for all the row addresses>

h)	WRT-A	0110	This is a dummy write, no bank is open, but it will increment the Y-counters. Do not increment the bank column

<repeat steps (a-h) for all the column addresses>

11) set the row and col counters to reverse direction, invert the data

	csb/ras/we/cas	<11,10,7,0>	
	PRE-ALL	1111	data inv=yes, Y=rev, X=rev
			No need to reload the XY scramble, just use the data invert mode again. (However, the XY scramble can be reloaded at any time the chip is idle to change the data pattern.)

12) Reset the row and col counters so a known starting point is valid.

	csb/ras/we/cas	<11,10,7,0>	
	BST	111x	row,col addresses = max bank col=00

13) Read the opposite data, row fast, reverse direction, modify the write data

	csb/ras/we/cas	<11,10,7,0>	
a)	ACT (4)	01xx	dec row address for next active
b)	NOP		
c)	READ0-NAP	1000	inc bank col for next read
d)	READ1-NAP	1000	inc bank col for next read
e)	READ2-NAP	1000	inc bank col for next read
f)	READ3-NAP	1000	inc bank col for next read
	NOPS(several)		
g)	WRT-A (4)	0100	no decrement, auto precharge,even start
	<repeat steps (a-g) for all the row addresses>		
h)	WRT-A	0110	This is a dummy write, no bank is open, but it will decrement the Y-counters. Do not increment the bank column
	<repeat steps (a-h) for all the column addresses>		

14) keep row and col counters in reverse direction, invert the data again.

	csb/ras/we/cas	<11,10,7,0>	
	PRE-ALL	1100	data inv=no, Y=rev, X=rev
			The data invert mode has been used again so the read data matches.

15) Read the original (twice inverted) data, row fast, reverse direction, no write

	csb/ras/we/cas	<11,10,7,0>	
a)	ACT (4)	01xx	dec row address for next active
b)	NOP		
c)	READ0-NAP	1000	inc bank col for next read
d)	READ1-NAP	1000	inc bank col for next read
e)	READ2-NAP	1000	inc bank col for next read
f)	READ3-AP	1100	inc bank col for next read
	<repeat steps (a-f) for all the row addresses>		
g)	WRT-A	0110	This is a dummy write, no bank is open, but it will decrement the Y-counters. Do not increment the bank column
	<repeat steps (a-g) for all the column addresses>		

END OF EXAMPLE #1

Test Example #2

Attached is an example of the test code needed to load and execute a pattern.
The following items are covered:

i)selecting the test modes based on the test's requirements
ii)selecting the desired cell matrix pattern and correlating it to the XY register.
iii) selecting which voltage supplies that need to be modulated for this particular test and correlating that to loading the VSR register.

iv) After loading the test registers, sample code is presented which indicates how the actual pattern may be run to obtain pass/fail information.

Example Test #2: Cell Margin Test, For Wafer Probe

TMRPAD (wafer probe)
TMR11MS will be used.
(TMCOMP and TMSCLK must be used since TMRPAD is used)
TMRDEN, Spares are tested (Row and Col)
TMSAOFB mode utilized
VINT and VBLH set using the ratio mode to 2.0/1.6V

Solid data pattern used

Data is "written" to the cells by toggling the wordlines while the VBLEQ voltage is at a level (= to the margin level) above VBLH/2.
TMSAOFB is used during the write, and the VBLEQ voltage must be varied.

The data is then read in normal fashion.
The TMSAOFB mode must be cancelled and the normal VBLEQ voltage re-enabled.

**Note ** This example does not represent any particular test that may actually be used. It is just an assembly of several different test modes to show by example how they may be used.

1) Set-up

X16VCC,DQ<7,8> should all be forced to 0V so the part is in TMRPAD
VCCX should be set to 2.5V so VINT and VBLH will be correct once VRATIO mode is entered.
The output strobe should be set for CL=2

2) Load the main test mode register, need modes <4,9,10,14,22,27> active

**intial emrs to enable test mode power can be skipped, because the part is already in TMRPAD by I/O configuration.

	csb/ras/we/cas	<11,10,7,0>	(reference MTR, table TM-B-1
	MRS	1010	Load enable command
	MRS	0011	Select to load Main Test Register
7 load cycles	MRS	0000	load modes <3:0>, none selected
V	MRS	0000	load modes <7:4>, none selected
V	MRS	0110	select modes <10,9>,TMRDEN,TMSCLK
	MRS	0100	select mode <14>, TMR11MS
	MRS	0000	load modes <19:16>, none selected
	MRS	0100	select mode <22>, TMCOMP
	MRS	10x0	load modes <27:24>, TMRPAD active by I/O configuration, so bit<25> is don't care.
	NOP		Need non-MRS command to cancel load sequence

3) Load the voltage set register, need VRAT mode, move VBLEQ +1 tick

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-3, "registers" sheet
	MRS	1010	Load enable command
	MRS	1011	Select to load Voltage Set Register
8 load cycles	MRS	0000	Vint control, set to default (VRAT will override)
V	MRS	0000	Vblh control, set to default (VRAT will override)
V	MRS	0000	Vpp control, set to default
	MRS	0000	Vpl control, set to default
	MRS	1000	set VBLEQ to .825mv (nominal is .8v), +1 tick
	MRS	0001	Vref=default Vrat control, see *** below
	MRS	0000	Vbb control, set to default
	MRS	0000	Vnwl control, set to default
	NOP		Need non-MRS command to cancel load sequence

*** bits <11,10> control VREF, also see table TM-D-1, "soft-set" sheet
VREF will automatically be generated by the chip since TMRPAD is active, it will default to the VREF=0.65*VINT value.

bits <7,0>="0","1" select VINT=.8*VCCX=2.0V (VCCX=2.5V)
VBLH=0.64*VCCX=1.6V

4) Load the XY scramble register, need solid "1"s pattern

The following diagram is porvided to help illustrate how the cell matrix will look with the intended pattern, and how it correlates to loading the register.

X0	>>		1	0	1	0	
X1	>>		0	0	1	1	
C1<0>		I/O <0>	I	I	I	I	A<11>
		I/O <2>	I	I	I	I	A<10>
		I/O <1>	I	I	I	I	A<7>
		I/O <3>	I	I	I	I	A<0>
C1<1>		I/O <1>	I	I	I	I	A<11>
		I/O <3>	I	I	I	I	A<10>
		I/O <0>	I	I	I	I	A<7>
		I/O <2>	I	I	I	I	A<0>

O=TRENCH POSITION = "0"

I=TRENCH POSITION = "1"

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-2, "registers" sheet
	MRS	1010	Load enable command
	MRS	0111	Select to load XY Register
4 load cycles	MRS	1111	X-read register, solid "1" pattern
V	MRS	xxxx	don't care for this test ****
V	MRS	0000	C1=0 register, no data, set for row stripe
	MRS	0000	C1=1 register, no data, set for row stripe
	NOP		Need non-MRS command to cancel load sequence

**** The Xwrite register is not used since the data is written by toggling the wordlines with sensing disabled and VBLEQ at an elevated voltage.

5) Enable the test modes

csb/ras/we/cas	<11,10,7,0>	
MRS	1111	enable the test modes

At this point all of the registers have been loaded for the initial pass, and the test modes are now active.

6) set the row and col counters to forward direction

	csb/ras/we/cas	<11,10,7,0>	
	PRE-ALL	0100	no data inv, Y=fwd, X=fwd

7) Reset the row and col counters so a known starting point is valid.

	csb/ras/we/cas	<11,10,7,0>	
	BST	111x	bank col, row,col addresses = 00000…

The solid internal "1"s can now be written.
Sensing has been disabled, and the VBLEQ voltage is slightly above VBLH/2.

Just running 4096+32=4128 refresh cycles will load all the cells with "1"s.

8) Write the background data, row fast, use REFs (4 bank parrallel)

	csb/ras/we/cas	<11,10,7,0>	
a)	REF	xxxx	
b)	NOP = several cycles		(satisfy TRFC, REF-REF delay)

<repeat steps (a-b) for all the row addresses,=4128 cycles>

At this point, prior to reading, sensing has to be re-enabled, and the VBLEQ voltage returned to normal.

9) Re-load the main test mode register, deactivate #27 (TMSAOFB)
**intial emrs to enable test mode power can be skipped, because the part is already in TMRPAD by I/O configuration.

	csb/ras/we/cas	<11,10,7,0>	(reference MTR, table TM-B-1
	MRS	1010	Load enable command (also deactivates)
	MRS	0011	Select to load Main Test Register
7 load cycles	MRS	0000	load modes <3:0>, none selected
V	MRS	0000	load modes <7:4>, none selected
V	MRS	0110	select modes <10,9>,TMRDEN,TMSCLK
	MRS	0100	select mode <14>, TMR11MS
	MRS	0000	load modes <19:16>, none selected
	MRS	0100	select mode <22>, TMCOMP
	MRS	00x0	#27 is now set to "0"
	NOP		Need non-MRS command to cancel load sequence

9-B) Alternate method of deactivating #27.
Since only #27 is changing, and it is the bottom row in the TM register, only 1 load command is needed. The other rows (bits 0-23) will remain unchanged.

	csb/ras/we/cas	<11,10,7,0>	(reference MTR, table TM-B-1
	MRS	1010	Load enable command
	MRS	0011	Select to load Main Test Register
1 load cycle	MRS	00x0	#27 is now set to "0"
	NOP		Need non-MRS command to cancel load sequence

10) Load the voltage set register, keep VRAT, return VBLEQ to normal

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-3, "registers" sheet
	MRS	1010	Load enable command
	MRS	1011	Select to load Voltage Set Register
8 load cycles	MRS	0000	Vint control, set to default (VRAT will override)
V	MRS	0000	Vblh control, set to default (VRAT will override)
V	MRS	0000	Vpp control, set to default
	MRS	0000	Vpl control, set to default
	MRS	0000	Vbleq control, set to default
	MRS	0001	Vref=default Vrat control, no change
	MRS	0000	Vbb control, set to default
	MRS	0000	Vnwl control, set to default
	NOP		Need non-MRS command to cancel load sequence

10-B) Alternate method of resetting VBLEQ only.
Since the VBLEQ line is the 4th row from the bottom, only 4 load commands are needed. Only the bottom 4 rows need to be loaded.

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-3, "registers" sheet
	MRS	1010	Load enable command
	MRS	1011	Select to load Voltage Set Register
4 load cycles	MRS	0000	Vbleq control, set to default
V	MRS	0001	Vref=default Vrat control, no change
V	MRS	0000	Vbb control, set to default
V	MRS	0000	Vnwl control, set to default
	NOP		Need non-MRS command to cancel load sequence

The data can now be read. TM4Bk mode is not used since we are reading only.
The ACT/READ commands can either be interleaved, or just done bank by bank. This example uses the interleave method.

The Xmax address is 1-C07h, and 4096+32=4128 total addresses/bank
The Ymax address is 1-10Ch, and 512+8=520 total addresses/bank
(h=address is in hex)
j-xxx where "j" denotes the spare address
<row counter should be at 0-000h after proper number of REF cycles>

12) Read the data, row fast, bank interleaved.

	csb/ras/we/cas	<11,10,7,0>	
a)	ACT0	10xx	inc bank_r address for next active, not row
b)	NOP		
c)	ACT1	10xx	inc bank_r address for next active, not row
d)	READ0-AP	1100	inc bank_col for next read
e)	ACT2	10xx	inc bank_r address for next active, not row
f)	READ1-AP	1100	inc bank_col for next read
g)	ACT3	11xx	inc bank_r and row address
h)	READ2-AP	1100	inc bank_col for next read
i)	NOP		
j)	READ3-AP	1100	inc bank_col for next read

<repeat steps (a-j) for all the row addresses, satisfy TRC for bank>

k)	WRT-A	0110	This is a dummy write, no bank is open, but it will increment the Y-counters. Do not increment the bank column. or, inc the col address for the last read from bank3 while incrementing the bank_col address.

<repeat steps (a-k) for all the column addresses>

END OF EXAMPLE #2

Test Example #3

Attached is an example of the test code needed to load and execute a pattern.
The following items are covered:

i)selecting the test modes based on the test's requirements
ii)selecting the desired cell matrix pattern and correlating it to the XY register.
iii) selecting which voltage supplies that need to be modulated for this particular test and correlating that to loading the VSR register.

iv) After loading the test registers, sample code is presented which indicates how the actual pattern may be run to obtain pass/fail information.

Example Test #3: Package Burn-in

TMCOMP
TMx1
TMSCLK (must be used since TMCOMP is used)
TMCBRUP

VINT=VCCX=2.8V, and VBLH=0.8xVCCX
VNWL ratio changed so -0.3V value kept despite fact VINT=2.8V
Checker data pattern used

write background
stress wordlines/cells for a while
read data

**Note ** This example does not represent any particular test that may actually be used. It is just an assembly of several different test modes to show by example how they may be used.

1) Set-up, Package

For X1 compression, data will be read on DQ<6>.
VCCX should be forced to 2.8V.
Tck should be slow, duty cycle should be very high for best efficiency of TMCBRUP

2) Load the main test mode register, need modes <7,9,22,23> active

	csb/ras/we/cas	<2,0>	
	EMRS	1,1	Enable Power to Test modes, DLL-OFF
	csb/ras/we/cas	<11,10,7,0>	(reference MTR, table TM-B-1
	MRS	1010	Load enable command
	MRS	0011	Select to load Main Test Register
7 load cycles	MRS	0000	load modes <3:0>, none selected
V	MRS	1000	load modes <7:4>, select <7>(TMCBRUP)
V	MRS	0110	select mode <9>, TMSCLK
	MRS	0000	load modes <15:12>, none selected
	MRS	0000	load modes <19:16>, none selected
	MRS	1100	select modes <22,23>, TMCOMP,TMX1
	MRS	0000	load modes <27:24>, none selected
	NOP		Need non-MRS command to cancel load sequence

3) Load the voltage set register, need VRAT mode, VNWL ratio change

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-3, "registers" sheet
	MRS	1010	Load enable command
	MRS	1011	Select to load Voltage Set Register
8 load cycles	MRS	0000	Vint control, set to default (VRAT will override)
V	MRS	0000	Vblh control, set to default (VRAT will override)
V	MRS	0000	Vpp control, set to default
	MRS	0000	Vpl control, set to default
	MRS	0000	Vbleq control, set to default
	MRS	0010	no VREF, VRAT (VINT=1x, VBLH=0.8x)
	MRS	0000	Vbb control, set to default
	MRS	0001	Vnwl control, =0.11xVINT
	NOP		Need non-MRS command to cancel load sequence

since this is a package test, default means read fuses.
**VBB fuses will probably have been blown to set VBB=0V

4) Load the XY scramble register, need checker pattern
initially set even wordlines (x0=0) to "1"

The following diagram is porvided to help illustrate how the cell matrix
will look with the intended pattern, and how it correlates to loading the register.

X0	>>		1	0	1	0	
X1	>>		0	0	1	1	
C1<0>		I/O <0>	**O**	**I**	**O**	**I**	A<11>
		I/O <2>	**I**	**O**	**I**	**O**	A<10>
		I/O <1>	**O**	**I**	**O**	**I**	A<7>
		I/O <3>	**I**	**O**	**I**	**O**	A<0>
C1<1>		I/O <1>	**O**	**I**	**O**	**I**	A<11>
		I/O <3>	**I**	**O**	**I**	**O**	A<10>
		I/O <0>	**O**	**I**	**O**	**I**	A<7>
		I/O <2>	**I**	**O**	**I**	**O**	A<0>

O=TRENCH POSITION = "0"

I=TRENCH POSITION = "1"

	csb/ras/we/cas	<11,10,7,0>	(reference VSR, table TM-B-2, "registers" sheet
	MRS	1010	Load enable command
	MRS	0111	Select to load XY Register
4 load cycles	MRS	0101	X-read register
V	MRS	0101	X-write register, =Xread
V	MRS	0101	C1=0 register, no data, set for column stripe
	MRS	0101	C1=1 register, no data, set for column stripe C1=A<1> Column Adress
	NOP		Need non-MRS command to cancel load sequence

**** combining a row and column stripe gives a checkerboard pattern.
Remember, the data for each trench is an EXOR of the active bit
(from either Read or Write line), and I/O that applies to that bit, from
the correct column register.

ex. What data is written/read when the address is X=1D6 and Y=B2 ?

ex. Row address 1D6h, only X1 and X0 matter, they are X1=1 and X0=0 for 0110 (6h).
In the cell matrix, this correponds to the last (4th) row.
It was loaded as a "1" for both the Xread and Xwrite lines of the XY register.

Col Address = B2h (X16 part), only C1 matters, and it is "1" for 0010 (2h)
Therefore the I/O data will be taken from the C1=1 line in the XY register.

		XR/XW data		C1=1 col data		Cell state
I/0 <0>	data=	"1"	exor	"0"	=	"1"
I/0 <1>		"1"		"0"	=	"1"
I/0 <2>		"1"		"1"	=	"0"
I/0 <3>		"1"		"1"	=	"0"

So, the cell states should match the intention of the cell matrix plan.

5) Enable the test modes

csb/ras/we/cas <11,10,7,0>

MRS 1111 enable the test modes

At this point all of the registers have been loaded for the initial pass, and the test modes are now active.

6) The first pass of the pattern can now be run.
Since TMRPAD is not being used, the pattern can be run with the tester in charge of all address pins.
At this point it becomes a normal test, except that no write data is being provided by the tester.
There is of course no read data either, just a single pass (=1) or fail (=0) on DQ<6> for each column address. Remember, rising and falling data are combined for x1 compression (DDR).
If it is an SDR part, the C0 address is a don't care.
(C11/C9 are always a don't care address for x4 or x1 compression.)

Since TMCBRUP mode is used. The internal wordline will be high as long as the external clock is high for a refresh cycle.

a) Do ACT/WRT/PRE cycles to write the data

b) do REF cycles to stress the wordlines and cells

c) do ACT/RED/PRE cycles to read (pass/fail) the data
<repeat (a,b,c) for all rows and columns

d) a PRE-ALL with A<11>=1 can be done to invert the data from the XY register.
<repeat (a,b,c) for opposite data>

END OF EXAMPLE #3

Revision History for D14TM# Document

Version	Date	Comments
D14TM0	1/15/2002	Initial release
D14TM1	1/17/2000	Corrected typo's, added some clarifications

This section (sheet in .xls file) is an example of the
Frequently Asked Questions, and hopefully the answers.
1/17/2002

Question: Where is the schematic TMBLK/TMINVREV or TMBLK/? ?

Answer: Schematics are not found here, they are in the 128D14 Schematics Notebook.
A full set of schematics is there for the whole chip.
There is also a .pdf file, 128D14_SCH.pdf which matches the notebook.

Question: How fast can the MRS registers be loaded?

Answer: In theory, they can be loaded as fast as the chip can run. The only limitation is that more set-up time may be needed for the addresses. This will have to be verified once the chip is initially tested.

Question: Why isn't VPP measured directly on the UDM pad in TMVEAS mode (instead of VPP/2)?

Answer: Since UDM is a true functional pad, there is a CMOS pass gate controlling whether to connect the pad to an internal voltage (for measuring), or to have it driven by UDM (functional).
To avoid ESD and Latch-up problems, this pass gate is controlled by VCCX and VSS levels.
Therefore, only voltages between VCCX and 0V can be measured with this test mode.
VNWL and VBB can only be monitored with their individual pads and thus can never be verified while in a package.
VPP/2 was the easiest choice to achieve some measure of VPP while in a package.
VPP of course also has an individual pad for wafer level, which will probably be used since several wafer tests require the use of forcing VPP, not just measuring it.

Qustion: Can the fuse ID information be read out in TMCOMP mode?

Answer: Yes and no.
To read fuse ID information the TMOUT mode must be set.
Once TMOUT is set, no data (real or compressed) can be read from the chip.
Only the signals as described for TMOUT mode can be read.
So, if TMCOMP or TMX1 is set while TMOUT is active, they are ignored.
(DQ<6> reads fuse info in TMOUT mode, not any type of data)
see sheet "DESC", page 10, TMOUT section.

G – ADDRESS / DATA SCRAMBLE

The attached diagrams map the following scrambles:

(for mapping failure addresses to physical location, i.e. making fail bit maps)

SCRAMR- the Row scramble, although there really is no row scramble for this part.

SCRCX16- Column scramble for x16 parts
SCRCX8- Column scramble for x8 parts
SCRCX4- Column scramble for x4 parts

A different column scramble is needed for each part, because of the way the C8 and C9 addresses are added for the x8 and x4 parts.
(C8=A8 column address, C98= decoded C9/C8 combinations <0:3>, C9=msb.)
This mapping was necessary to facilitate a compression test mode that also supported pre-fuse wafer repair, without adding yet another data path/mux to the chip!

DATA SCRAMBLE

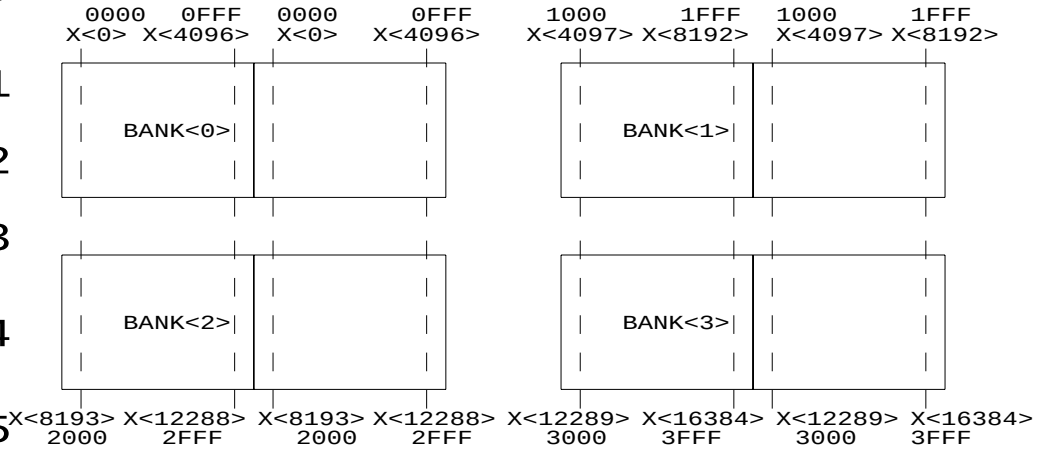
SCRDX16- Data scramble for x16 parts, even I/Os fit one equation, odd I/Os are the inverse.
SCRDX8- These are of course the same I/O paths used in a X16 chip, using a column address (Y1) and row address (X1) you must determine if you are in an odd or even I/O location.
SCRDX4-Similar to the X8 data scramble, just a little different.

Notes:
We will verify these scrambles with the first wafer we receive.

ROW - ADDRESS SCRAMBLE FOR 128D14 DDR/SDR

(THERE IS NONE)

PHYSICAL		LOGICAL
X0		A0
X1		A1
X2		A2
X3		A3
X4		A4
X5		A5
X6		A6
X7		A7
X8		A8
X9		A9
X10		A10
X11		A11
X12	(BANK ADDRESS)	BA<0>
X13	(BANK ADDRESS)	BA<1>

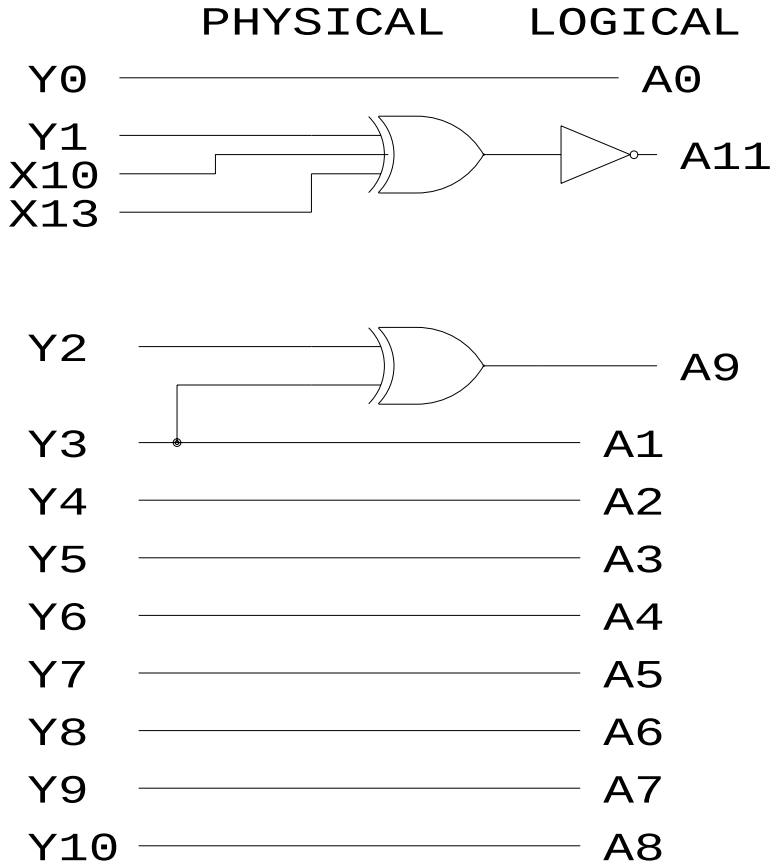


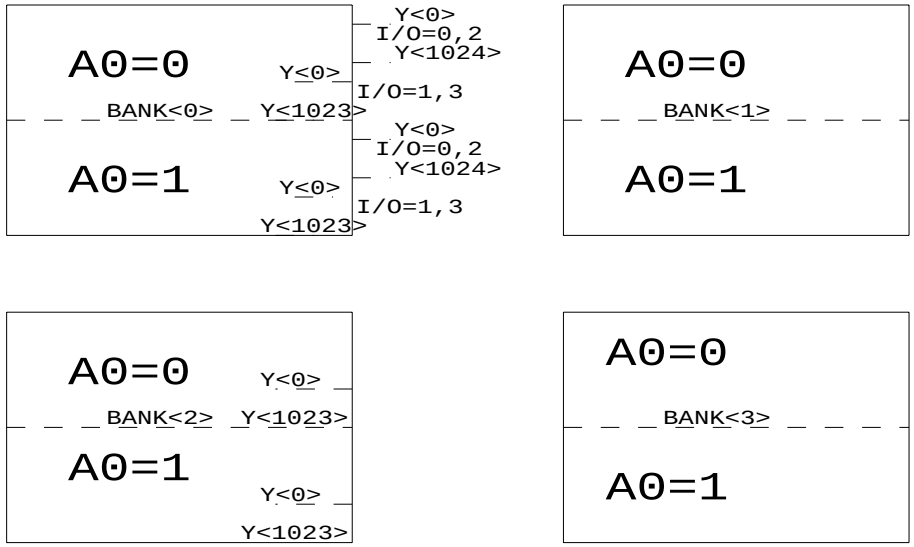
RIGHT AND LEFT HALF OF EACH BANK IS REPEATED

(EACH ROW ADDRESS CORRESPONDS WITH 2 ROWS/BANK)

UNITED MEMORIES INC. PROJECT: 128D14		
Title ROW - ADDRESS SCRAMBLE		
Size A	Document Number SCRAMR	REV A
Date: December 12, 2001	Sheet 1 of 1	

COLUMN ADDRESS SCRAMBLE FOR 128D14 DDR/SDR (X4)





THE PHYSICAL MAPPING OF A0 IS DIFFICULT,
IT WANTS TO BE Y10, THE MSB AS IT RELATES TO PHYSICAL POSITION/BITMAP.

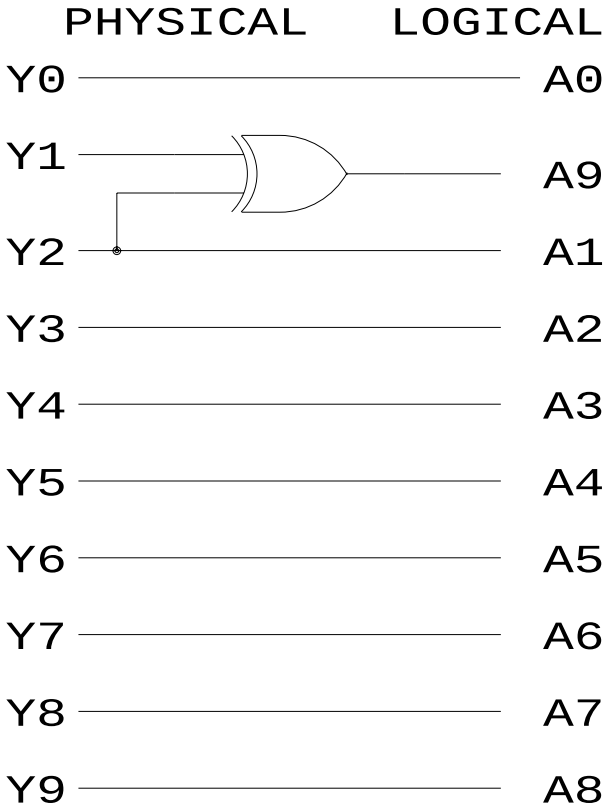
HOWEVER, IT MUST BE THE LSB AS FAR AS COUNTING AND DATA GENERATION.

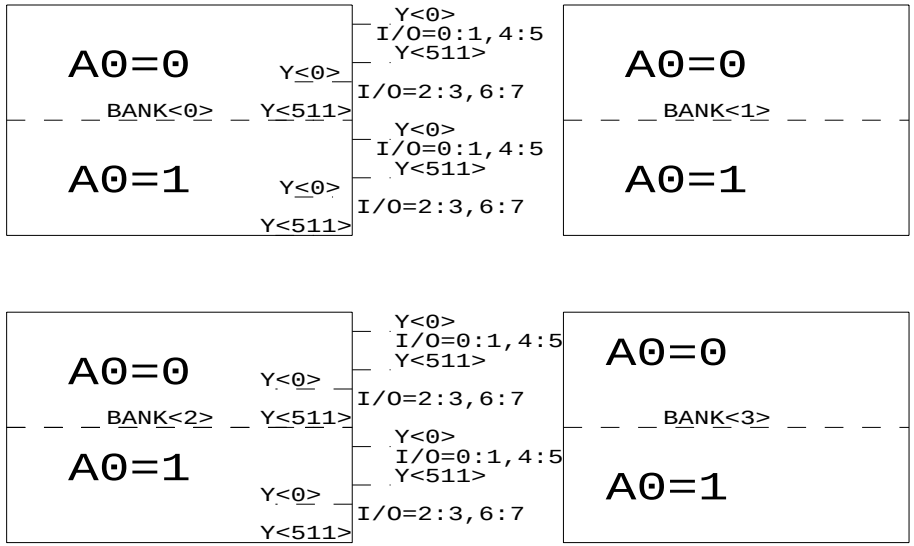
NO MATTER WHAT THE STARTING ADDRESS IS, A0 ALWAYS TOGGLES
BETWEEN THE RISING/FALLING DATA.

REM-THERE ARE 4 Y-SELECTS ACTIVE PER CYCLE,
TWO EACH FOR ODD AND EVEN DATA.

UNITED MEMORIES INC. PROJECT: 128D14		
Title X4 - COLUMN ADDRESS SCRAMBLE		
Size A	Document Number SCRCX4	REV A
Date: December 12, 2001	Sheet 1 of 1	

COLUMN ADDRESS SCRAMBLE FOR 128D14 DDR/SDR (X8)





THE PHYSICAL MAPPING OF A0 IS DIFFICULT,
IT WANTS TO BE Y9, THE MSB AS IT RELATES TO PHYSICAL POSITION/BITMAP.

HOWEVER, IT MUST BE THE LSB AS FAR AS COUNTING AND DATA GENERATION.

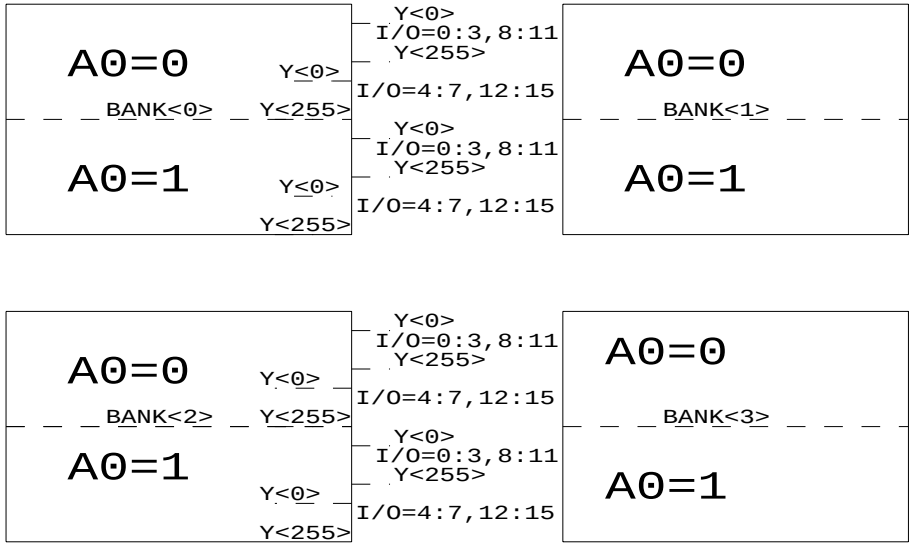
NO MATTER WHAT THE STARTING ADDRESS IS, A0 ALWAYS TOGGLES
BETWEEN THE RISING/FALLING DATA.

REM-THERE ARE 4 Y-SELECTS ACTIVE PER CYCLE,
TWO EACH FOR ODD AND EVEN DATA.

UNITED MEMORIES INC. PROJECT: 128D14		
Title X8 - COLUMN ADDRESS SCRAMBLE		
Size A	Document Number SCRCX8	REV A
Date: December 12, 2001	Sheet 1 of 1	

COLUMN ADDRESS SCRAMBLE FOR 128D14 DDR/SDR (X16)

PHYSICAL	LOGICAL
Y0	A0
Y1	A1
Y2	A2
Y3	A3
Y4	A4
Y5	A5
Y6	A6
Y7	A7
Y8	A8



THE PHYSICAL MAPPING OF A0 IS DIFFICULT,
IT WANTS TO BE Y7, THE MSB AS IT RELATES TO PHYSICAL POSITION/BITMAP.

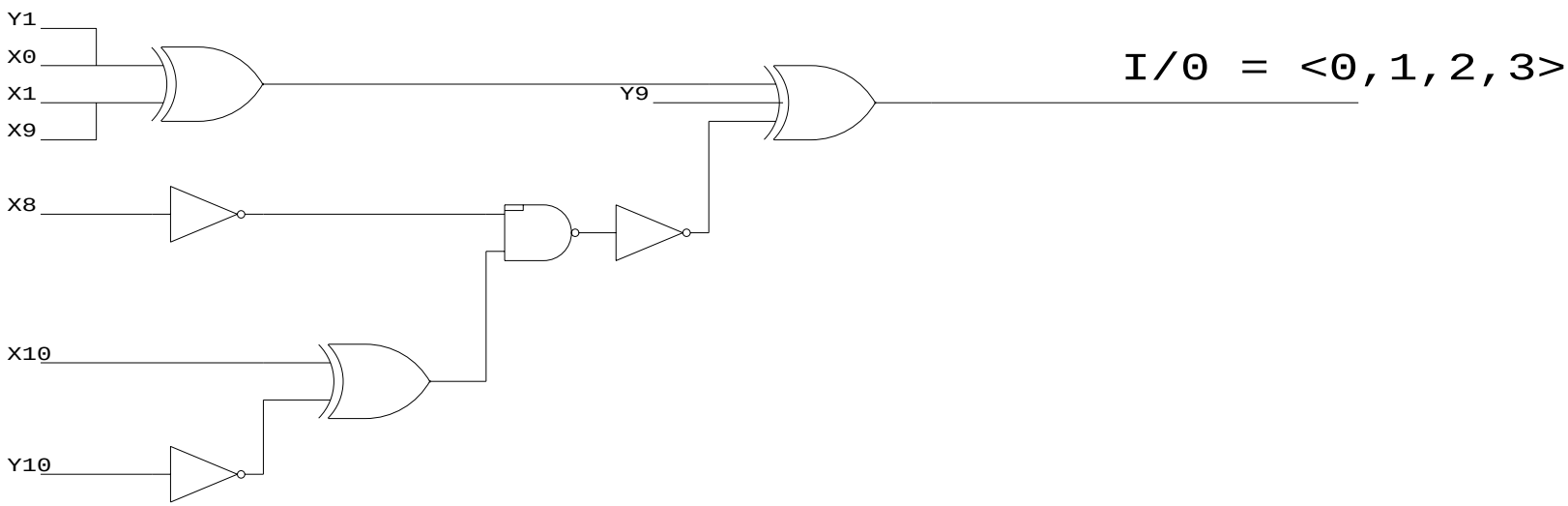
HOWEVER, IT MUST BE THE LSB AS FAR AS COUNTING AND DATA GENERATION.

NO MATTER WHAT THE STARTING ADDRESS IS, A0 ALWAYS TOGGLES
BETWEEN THE RISING/FALLING DATA.

REM-THERE ARE 4 Y-SELECTS ACTIVE PER CYCLE,
TWO EACH FOR ODD AND EVEN DATA.

UNITED MEMORIES INC. PROJECT: 128D14		
Title COLUMN ADDRESS SCRAMBLE - X16		
Size A	Document Number SCRCX16	REV A
Date: December 12, 2001	Sheet 1 of 1	

DATA SCRAMBLE FOR X4 128D14 DDR/SDR



NOTE: A11 ON DUT IS Y10 ON TESTER.

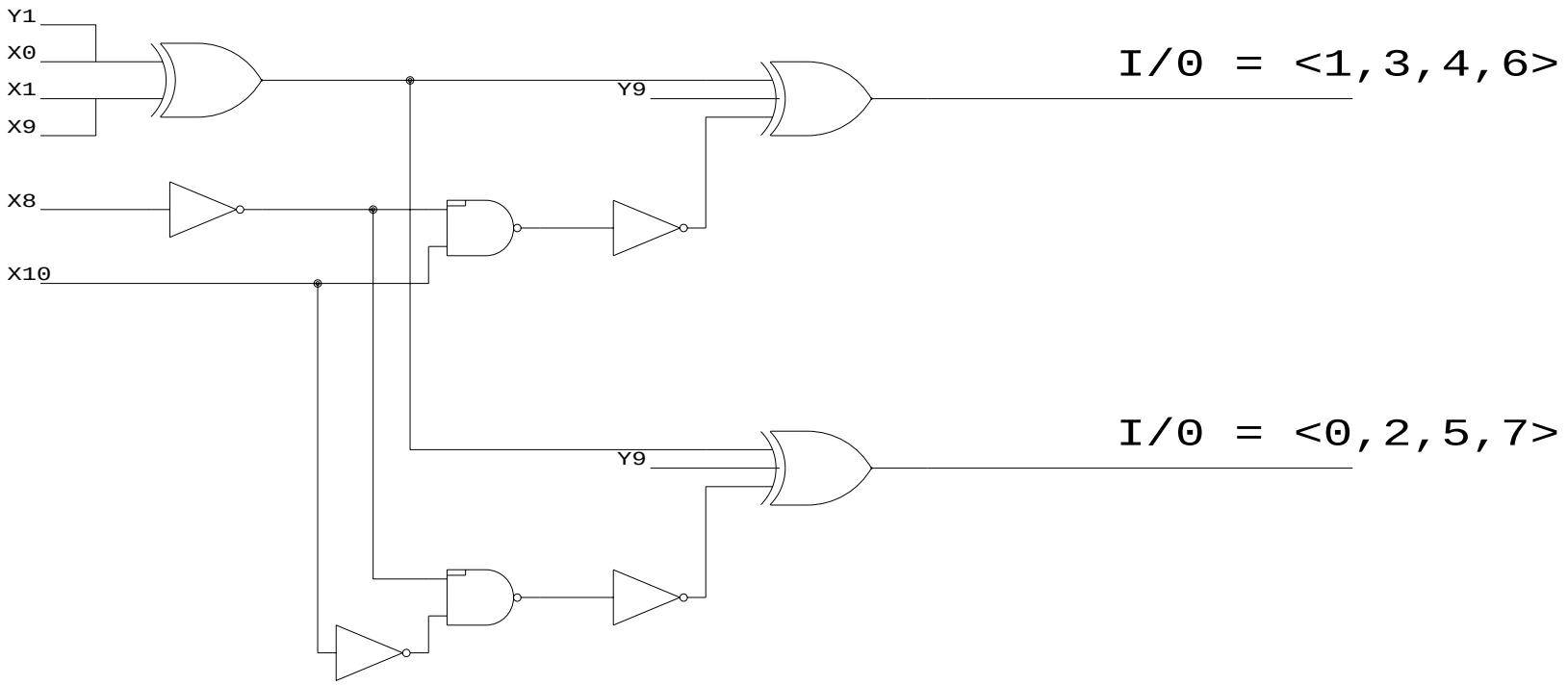
"1"=INVERT

	C119	<0>	<1>	<2>	<3>
L-BYTE	IO	<0>	<1>	<2>	<3>
	IO	<4>	<5>	<6>	<7>
U-BYTE	IO	<11>	<10>	<9>	<8>
	IO	<15>	<14>	<13>	<12>
		X8		X8 X4 CTM	

FOR X4, USE Y9 AND Y10

UNITED MEMORIES INC. PROJECT: 128D14		
Title X4 - DATA SCRAMBLE		
Size A	Document Number SCRDX4	REV A
Date: December 12, 2001	Sheet 1 of 1	

DATA SCRAMBLE FOR X8 128D14 DDR/SDR



"1"=INVERT

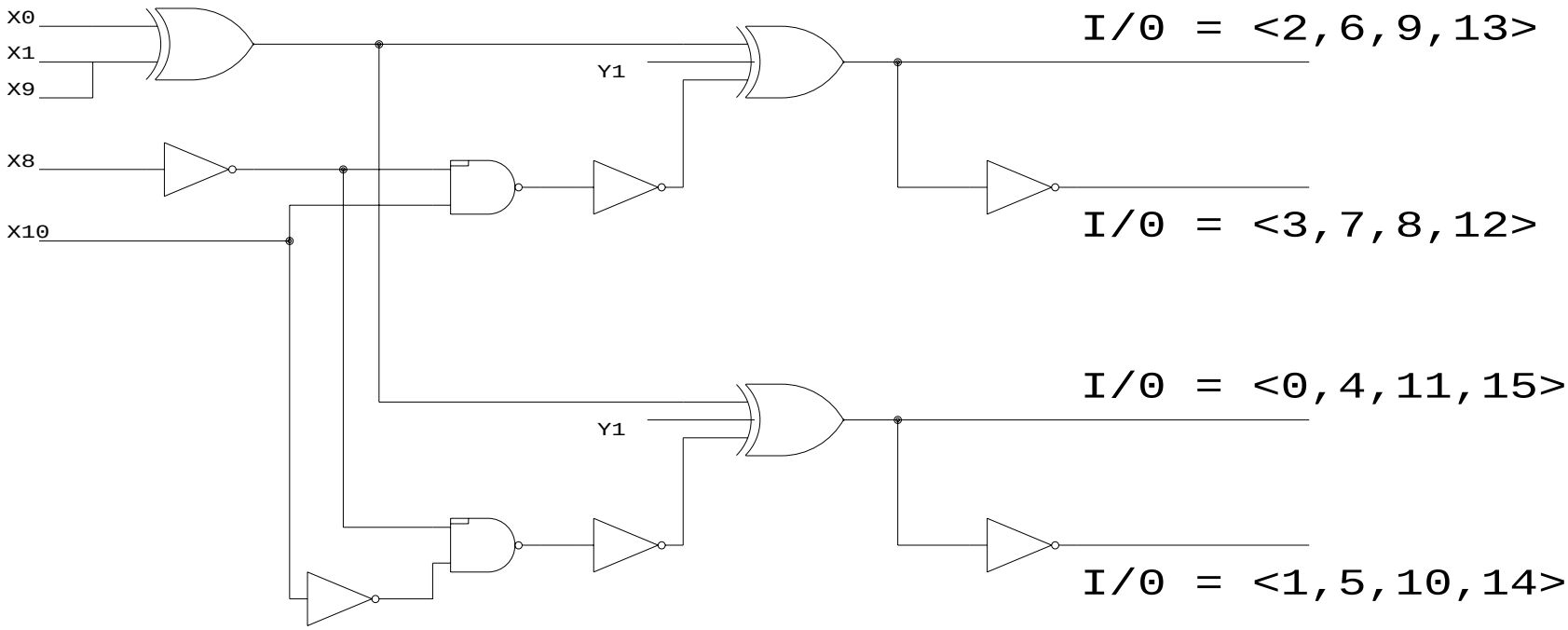
	C119	<0>	<1>	<2>	<3>
L-BYTE	IO	<0>	<1>	<2>	<3>
	IO	<4>	<5>	<6>	<7>
U-BYTE	IO	<11>	<10>	<9>	<8>
	IO	<15>	<14>	<13>	<12>

X8 X8
X4
CTM

FOR X8, USE Y9 ADDRESS
NO A11 COLUMN ADDRESSES

UNITED MEMORIES INC. PROJECT: 128D14		
Title X8 - DATA SCRAMBLE		
Size A	Document Number SCRDX8	REV A
Date: December 12, 2001	Sheet 1 of 1	

DATA SCRAMBLE FOR X16 128D14 DDR/SDR



"1"=INVERT

	C119	<0>	<1>	<2>	<3>
L-BYTE	IO	<0>	<1>	<2>	<3>
	IO	<4>	<5>	<6>	<7>
U-BYTE	IO	<11>	<10>	<9>	<8>
	IO	<15>	<14>	<13>	<12>

X8 X8
X4
CTM

FOR X16 / ALL ON
NO A9,A11 COLUMN ADDRESSES

UNITED MEMORIES INC. PROJECT: 128D14		
Title X16 - DATA SCRAMBLE		
Size A	Document Number SCRDX16	REV A
Date: December 12, 2001	Sheet 1 of 1	

H – FUSE DESCRIPTIONS

Attached are fuse diagrams and tables for:

ROW Fuses

Column Fuses

VDC Programming Fuses
(VINT, VINT DLL, VREF)

VPP Programming Fuses

VBB Programming Fuses

VNWL Programming Fuses

The Row and Column Fuses are based on the same concept.

Each spare element has a unique address to allow for pre-fuse testing.
If you desire to use that element,
First blow its enable fuse,
Then blow the fuse of any address bit that doesn't match its default.

The attached text and diagrams explain this is detail.

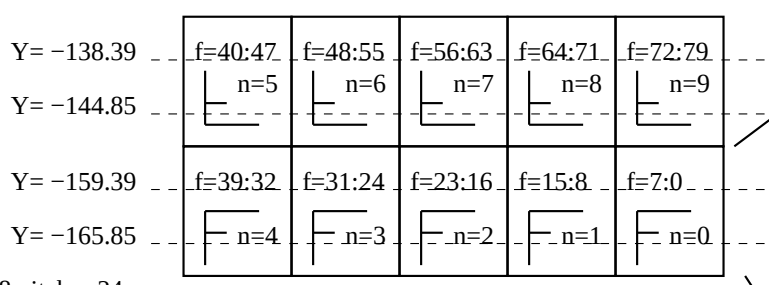
Total redundancy is as follows:

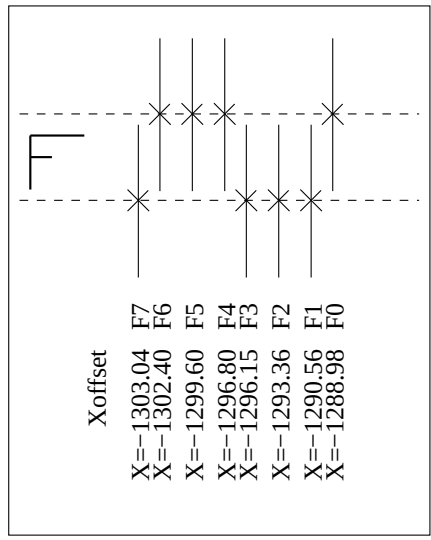
For Rows, 8 spare rows located per 4Meg sub-array.
Only 1 row is deleted/added per element.
There is no jumping of 4M sub-arrays.
Should be no difference in access time for reals and spares (they are both slow!)
A fuse set "pulse" is fired everytime the bank goes active, only 1 pulse is needed, but relying on a single pulse at power-up seemed risky.

The columns are a little tricky.
A bank is divided into 4 horizontal quadrants (HQUADS). Each HQUAD has 8 I/Os associated with it. Within the HQUAD there are 4 spare columns available for use.
All 8 I/Os are swapped out with each spare Y.
Each spare Y can have two separate addresses, one for R11=0, the other for R11=1.
A spare –Y can ONLY be used twice if the R11 address is different.

ID FUSE LOCATIONS

12/10/01





f0 to f8 pitch = 24

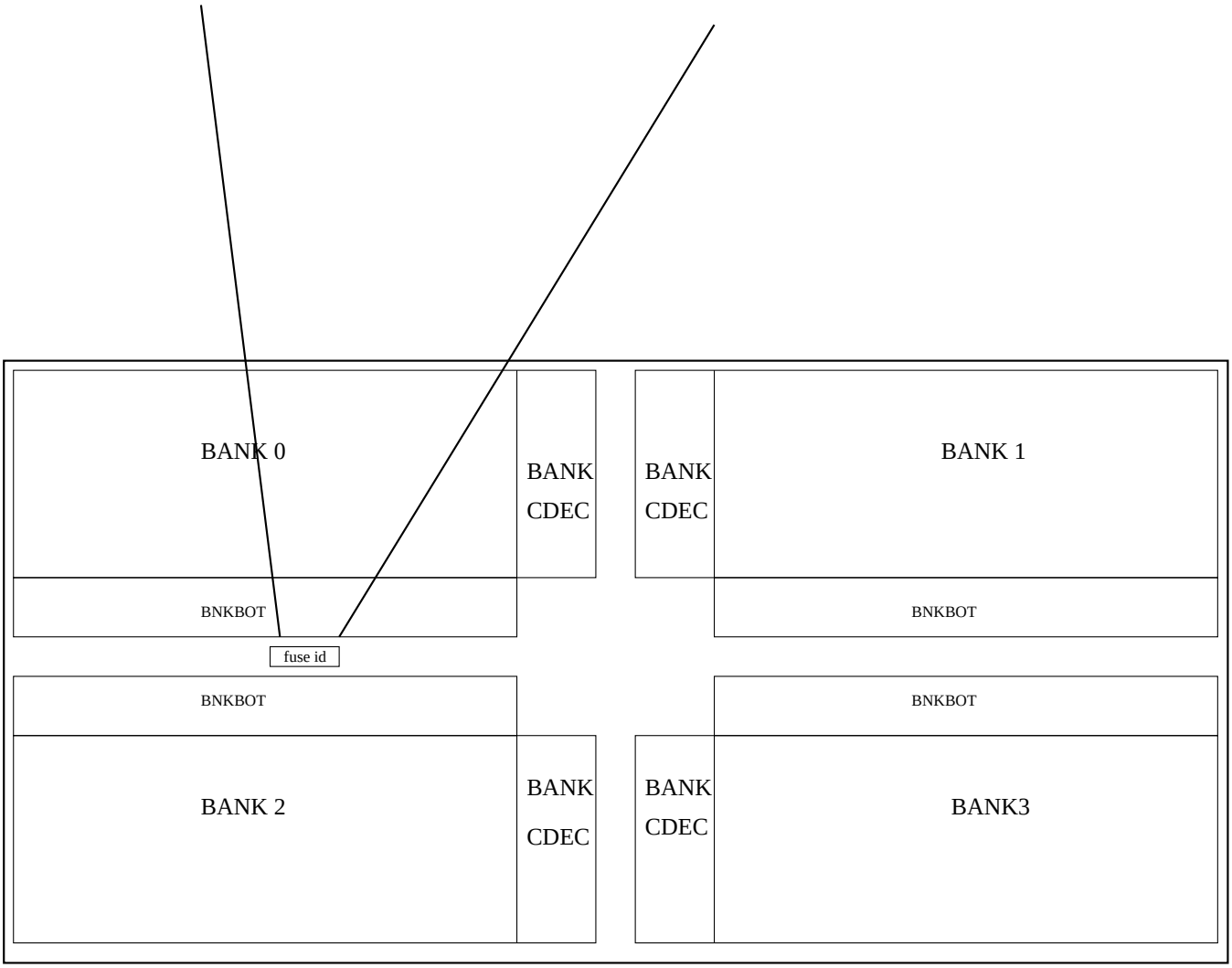
for f <= 39 X(fn)= Xoffset − n(24) (n=0:4)

Y(f + 8n)=−159.39 for f=0,4,5,6
Y(f + 8n)=−165.85 for f=1,2,3,7

for f>39 X(fn)= Xoffset − 216 + 24n (n=5:9)

Y(f + 8n)=−144.85 for f=0,4,5,6
Y(f + 8n)=−138.39 for f=1,2,3,7

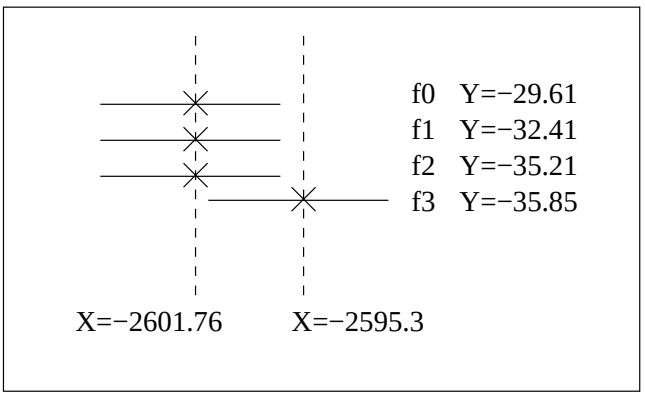
Note: fuse number = f + 8n

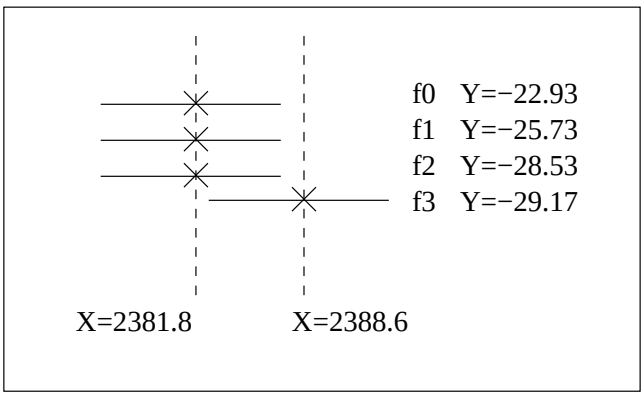


fuseid.fig

128D14 VPP fuse locations

12/10/01

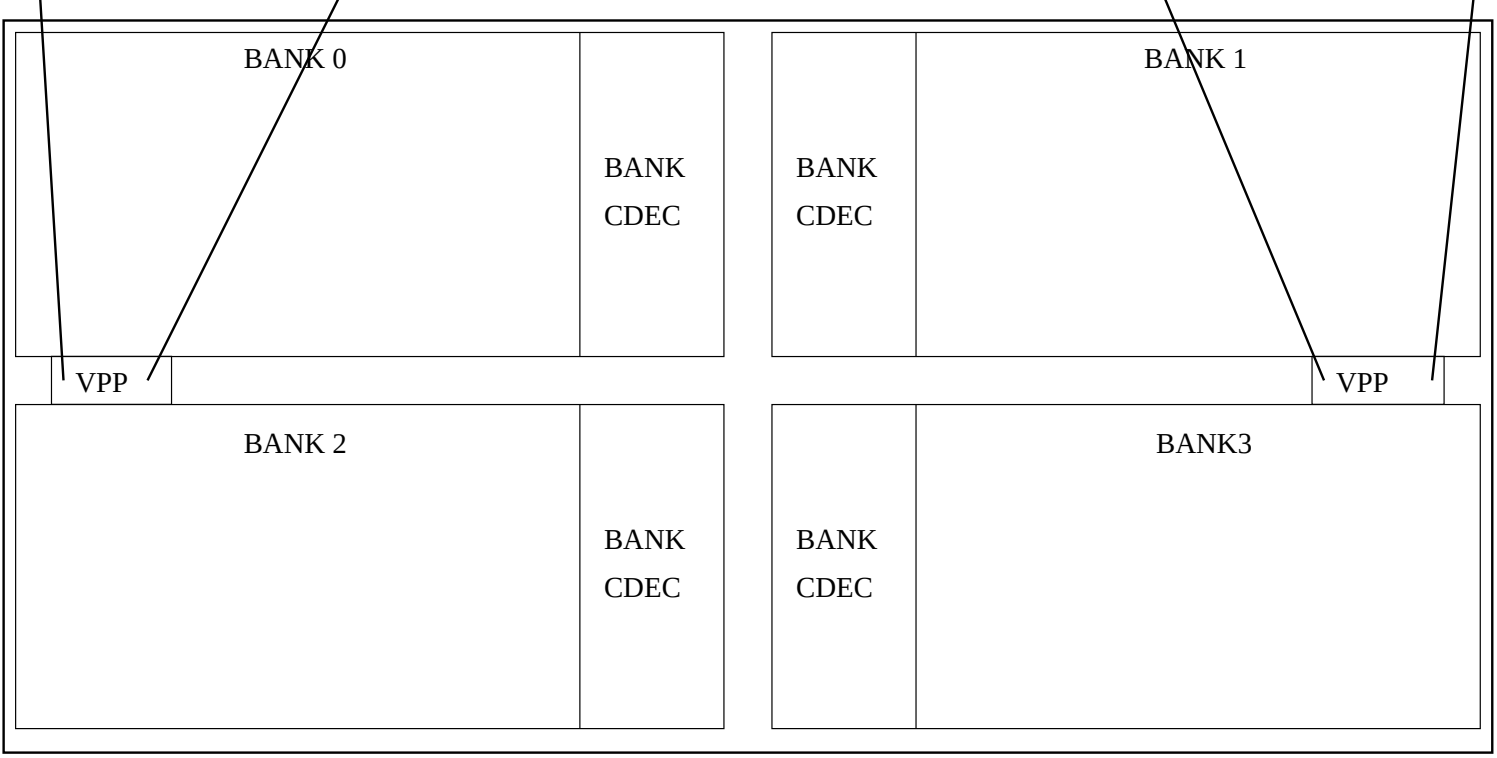




Refer to VPP schematic

f(0) → T(0)
f(1) → T(1)
f(2) → T(2)
f(3) → T(3)

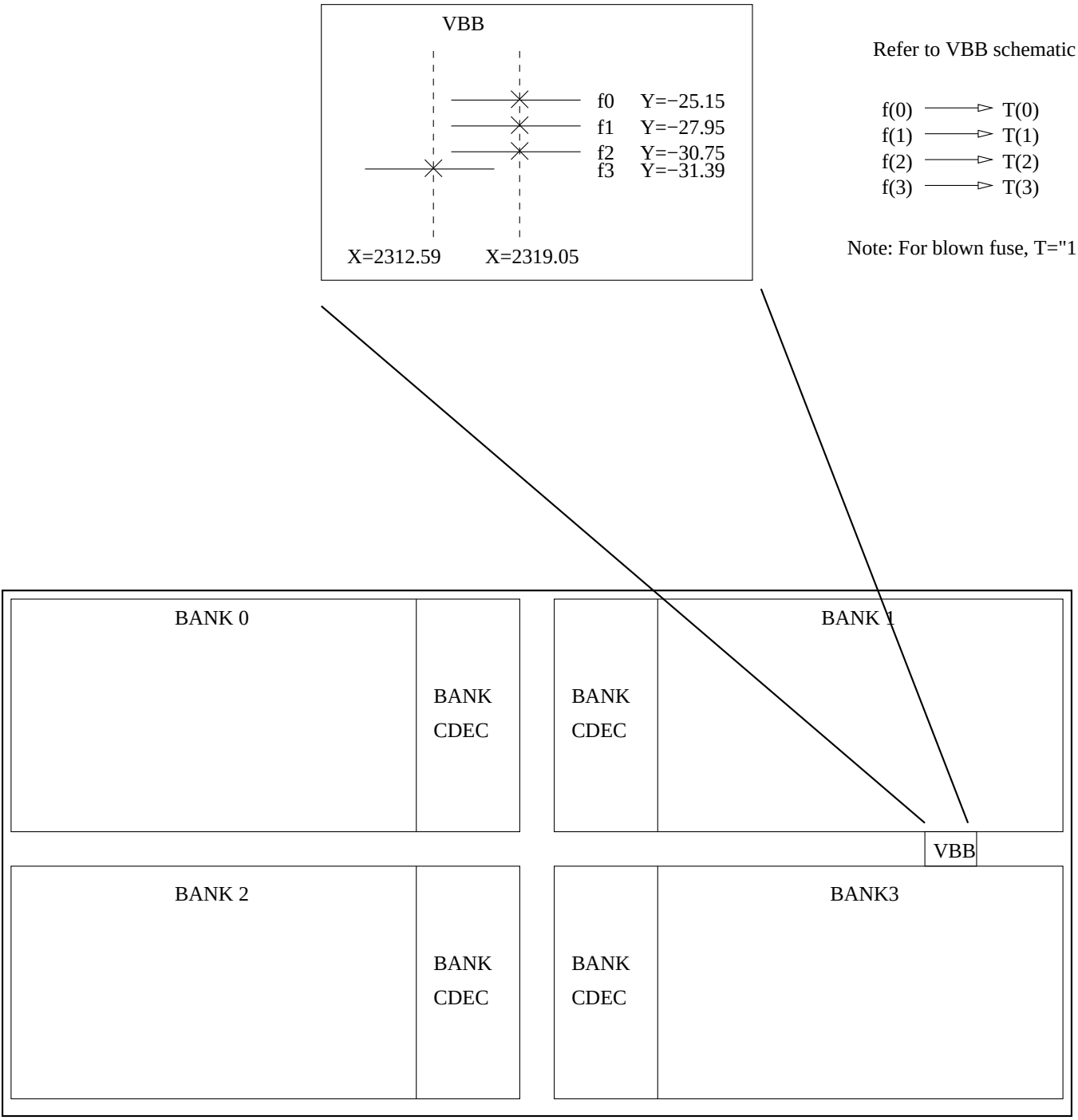
Note: For blown fuse, T="1"



vppfusloc.fig

128D14 VBB fuse locations

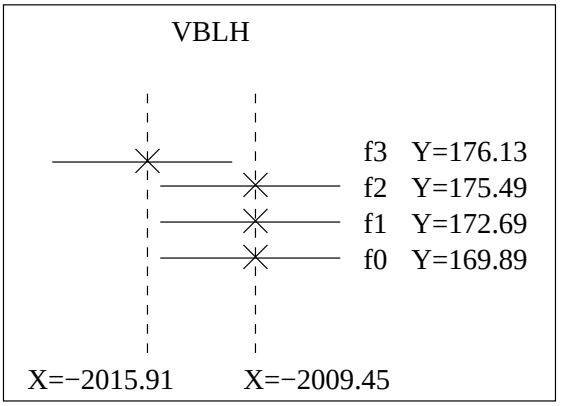
12/10/01

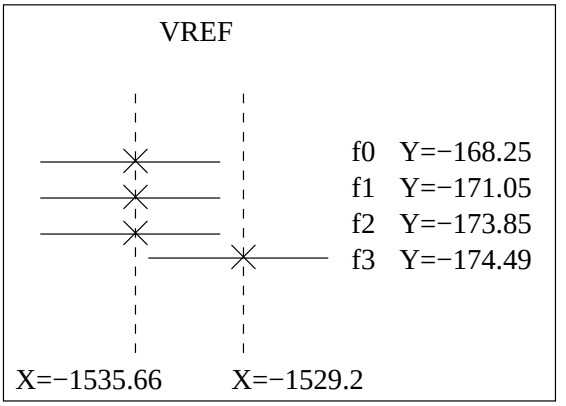


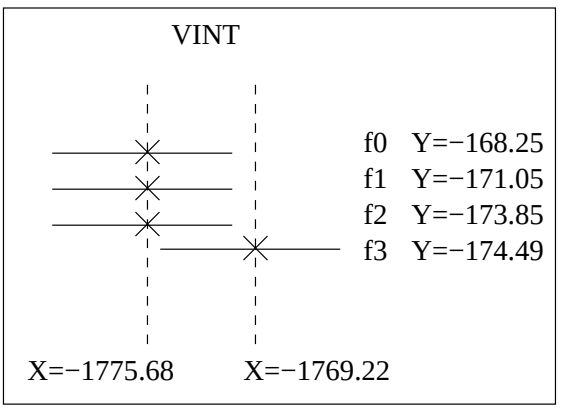
vbbfusloc.fig

VDC fuse locations

12/10/01



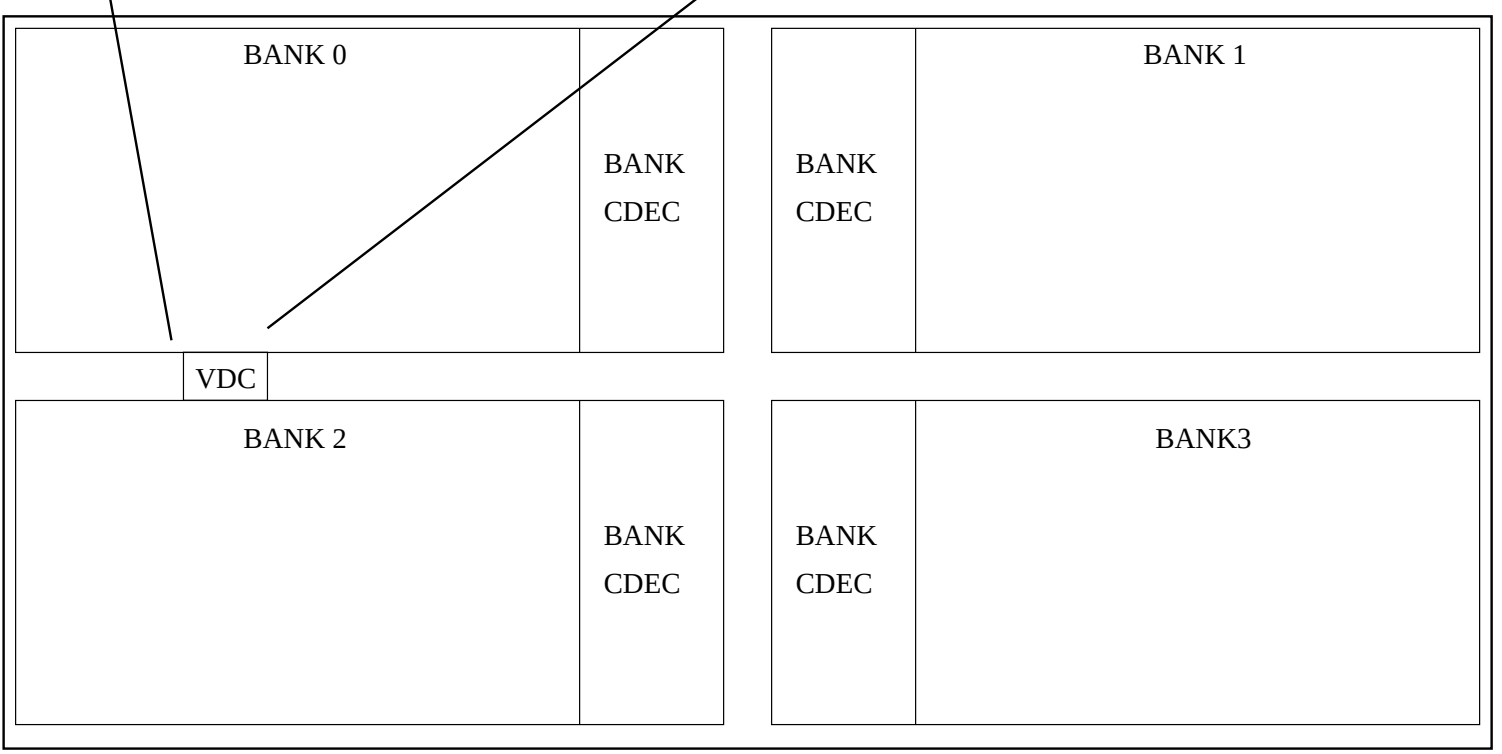




Refer to VDC schematic

f(0) → T(0)
f(1) → T(1)
f(2) → T(2)
f(3) → T(3)

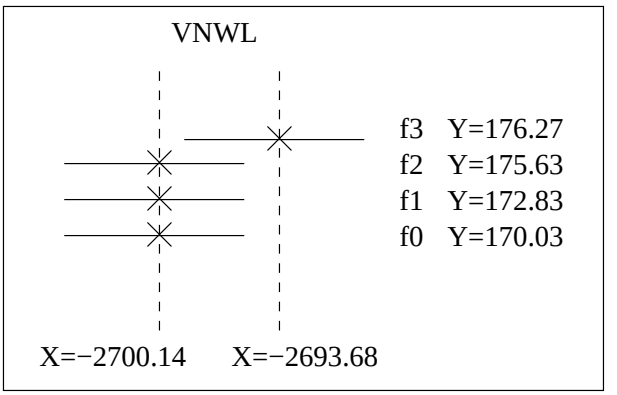
Note: For blown fuse, T="1"



vdcfusloc.fig

VNWL fuse locations

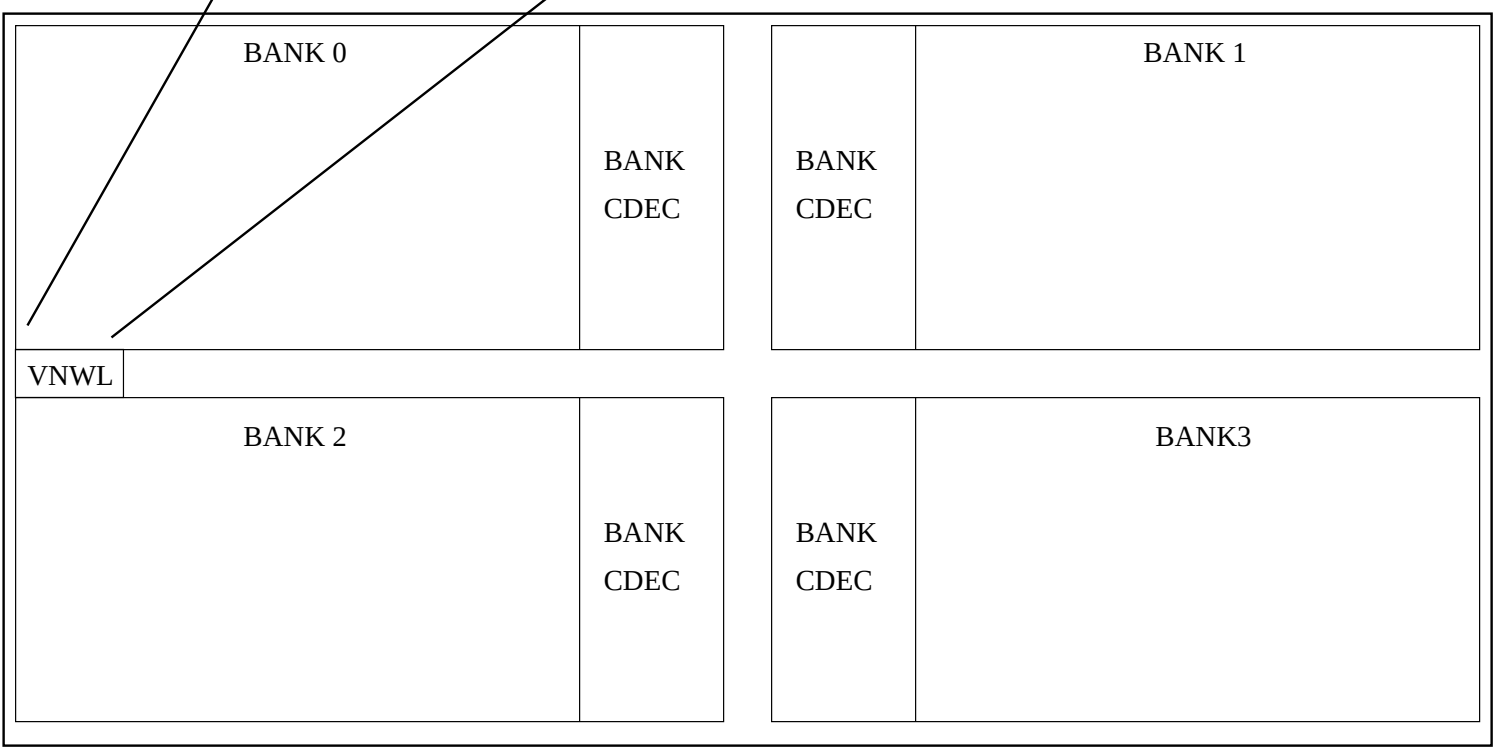
12/10/01



Refer to vnwlgen schematic

f(0) → T(0)
f(1) → T(1)
f(2) → T(2)
f(3) → T(3)

Note: For blown fuse, T="1"



vnwlfusloc.fig

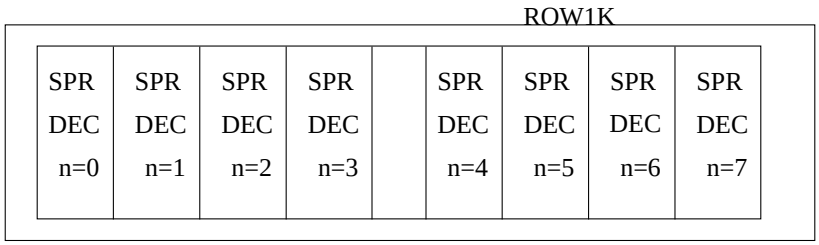
128D14 SPARE ROW DECODER FUSE LOCATIONS

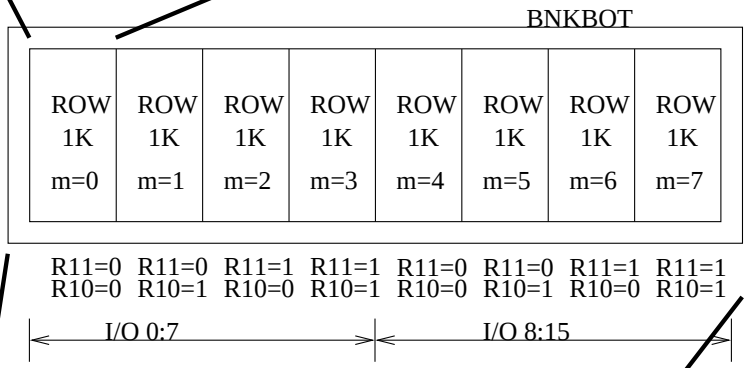
12/10/01

SPRDEC PITCH=34.68

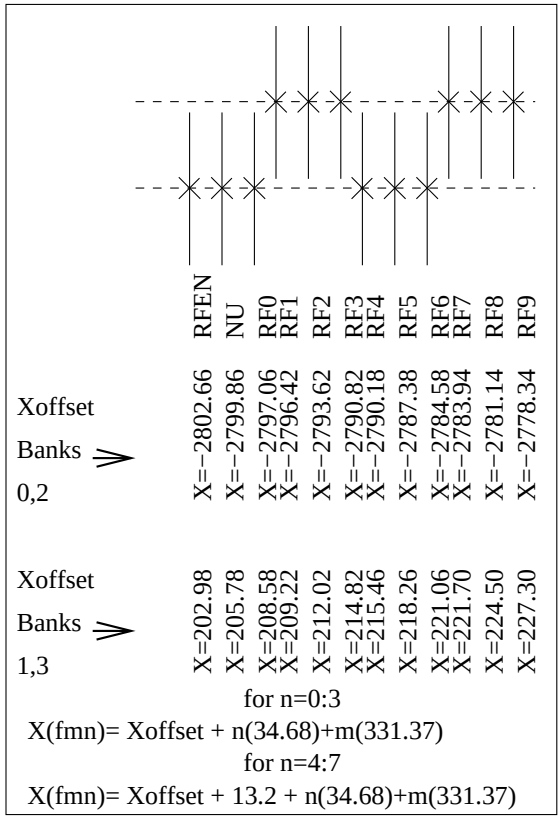
(n=0,4) PITCH=151.92

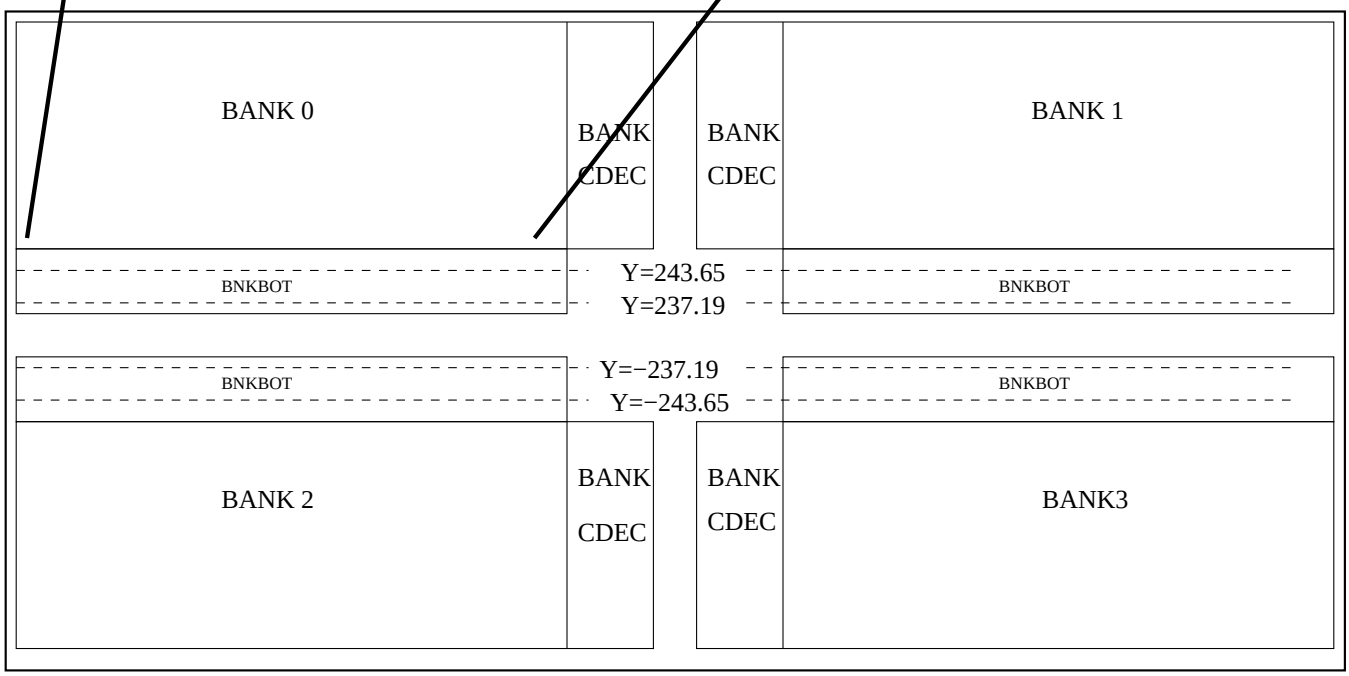
ROW1K PITCH=331.37





SPRDEC





rowfusloc.fig

The following description refers to the RFUSE schematic, the SPRDEC schematic and the ROW DECODER FUSE LOCATIONS document.

The row redundancy for the 128D14 consists of 64 spare row decoders per bank, with the chip containing a total of 4 banks. Each bank contains 8 sub-blocks labeled ROW1K. Each ROW1K contains 8 spare row decoders labeled SPRDEC. Each SPRDEC contains a total of 11 fuses which results in a total of 704 fuses per bank. It should be noted that 1 SPRDEC enables 1 row. The 8 spare row decoders in a given ROW1K block can only repair rows within that block. Note: In the layout, there are actually 12 fuses in each SPRDEC, but only 11 are used.

The schematic RFUSE contains 88 fuses representing the 8 spare row decoders in ROW1K. The fuses are labeled RF(n)X where n is the spare decoder number (0:7) and X is the fuse number (0:9). The enable fuses are labeled RFEN(X) where X is once again, the spare decoder number. A description of the fuses is as follows:

Fuses RFEN<0:7> are enable fuses which are used to enable the selected spare row decoder. Fuses RF(n)(0:9), which will now be referred to as RF0 - RF9 by dropping the spare decoder number, allow for programming with the row address information R0-R9. Note that R10 and R11 are used to decode which ROW1K block is selected (See SPARE ROW FUSE LOCATIONS sheet). A given combination of R10 and R11 occurs twice within a BNKBOT. The distinction between the two occurrences is determined by I/O number. For BANKS 0 and 1, I/O(0:7) is controlled by ROW1K(m=0:3), I/O(8:15) is controlled by ROW1K(m=4:7). For BANKS 2 and 3, I/O(0:7) is controlled by ROW1K(m=4:7) and I/O(8:15) is controlled by ROW1K(m=0:3).

In order to repair a bad row, the enable fuse is blown to select the desired spare row decoder. Next, the address is programmed by blowing fuses RF3-RF9 where a "1" appears for a given address bit. RF0-RF2 must be programmed based on the table in the schematic SPRDEC. These 3 address bits enable pre-fuse testing of the 8 spare row decoders by assigning a unique address to each spare decoder. In order to program these three bits, a comparison must be done between the 3 address bits of the row to be replaced and the default address as given in the table. If a "1" appears in the table and the row address has a "1" in the same position, no fuse must be blown. If, however, a "0" appears in the table and the row address has a "1" in the same position, the fuse must be blown to program a "1".

The diagram on the ROW DECODER FUSE LOCATIONS shows the order and the X coordinate offset for the fuses in SPRDEC. Note that 2 sets of numbers are given. The first set of numbers is to be used for fuses in banks 0 and 2 and the second set is to be used for fuses in banks 1 and 3.

An example of programming a spare row dec is as follows:

```
                          11 10 9 8 7 6 5 4 3 2 1 0
Assume I/O 9, row address  1  0 1 1 0 0 1 1 0 1 0 1 in Bank 2 is failing.
```

Step 1: Determine which 4 meg block is failing.

with R11=1 and R10=0 and I/O 9 failing, block ROW1K with m=2 is the failing block.

Step 2: Choose a spare row decoder.

for this example, SPRDEC with n=4 is chosen.
BLOW FUSE RFEN4 in schematic RFUSE.

Step 3: Refer to SPRDEC schematic for row addresses A2-A0.

Since the decoder with n=4 was chosen, the default A2-A0 address is 100 (A2=1,A1=0,A0=0). Comparing this default address to the same bits in the failing address yields a difference in A0. This indicates that the fuse corresponding to A0 must be blown.
BLOW FUSE RF40 in schematic RFUSE.

Step 4: Program remaining bits in address field.

Blow fuses corresponding to A9 A8 A5 A4.

BLOW FUSES RF49 RF48 RF45 RF44.

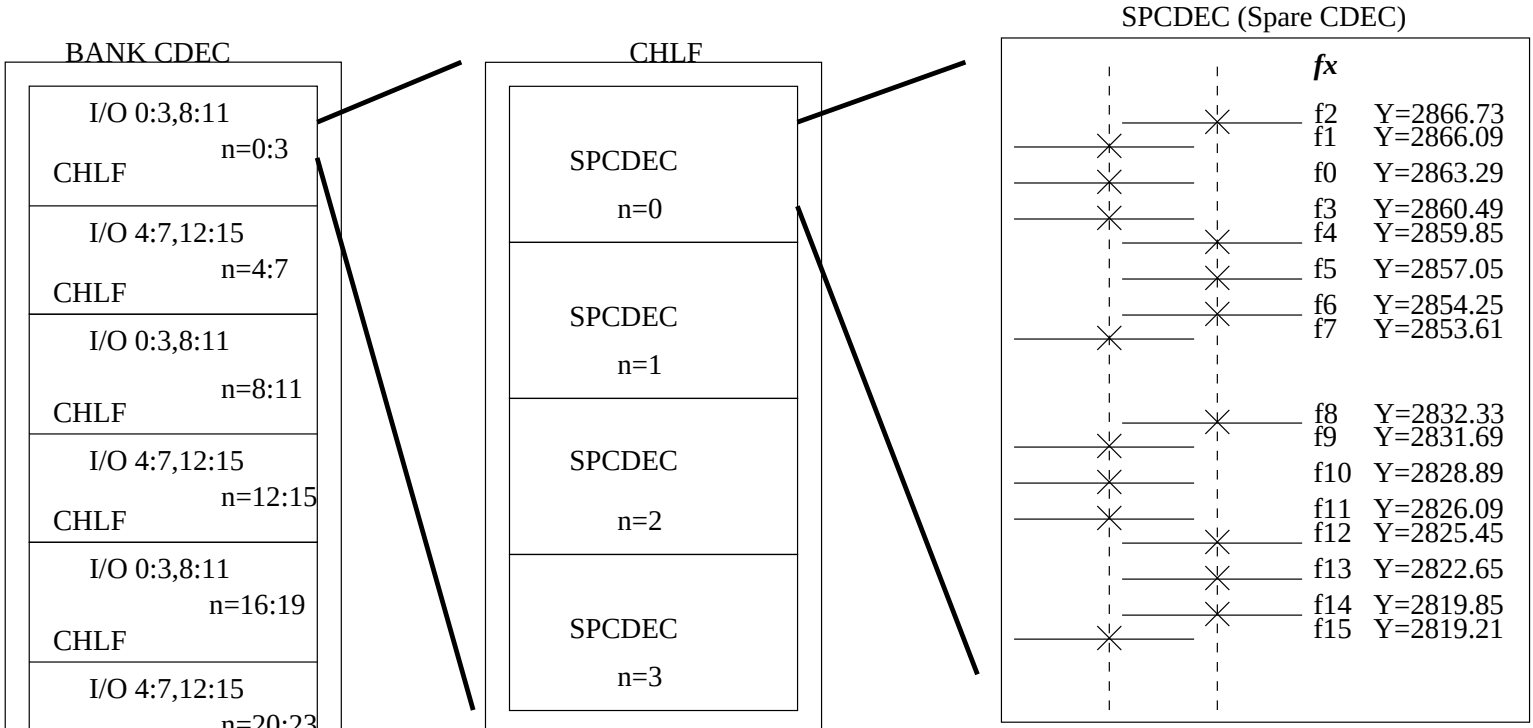
The X coordinates of the fuses are determined by the equation:

$$X(fmn)=Xoffset + 13.2 + n(34.68) + m(331.37)$$

where Xoffset is given in the table for each fuse in the SPRDEC.
m and n are as defined above.

128D14 SPARE COLUMN DECODER FUSE LOCATIONS

12/10/01

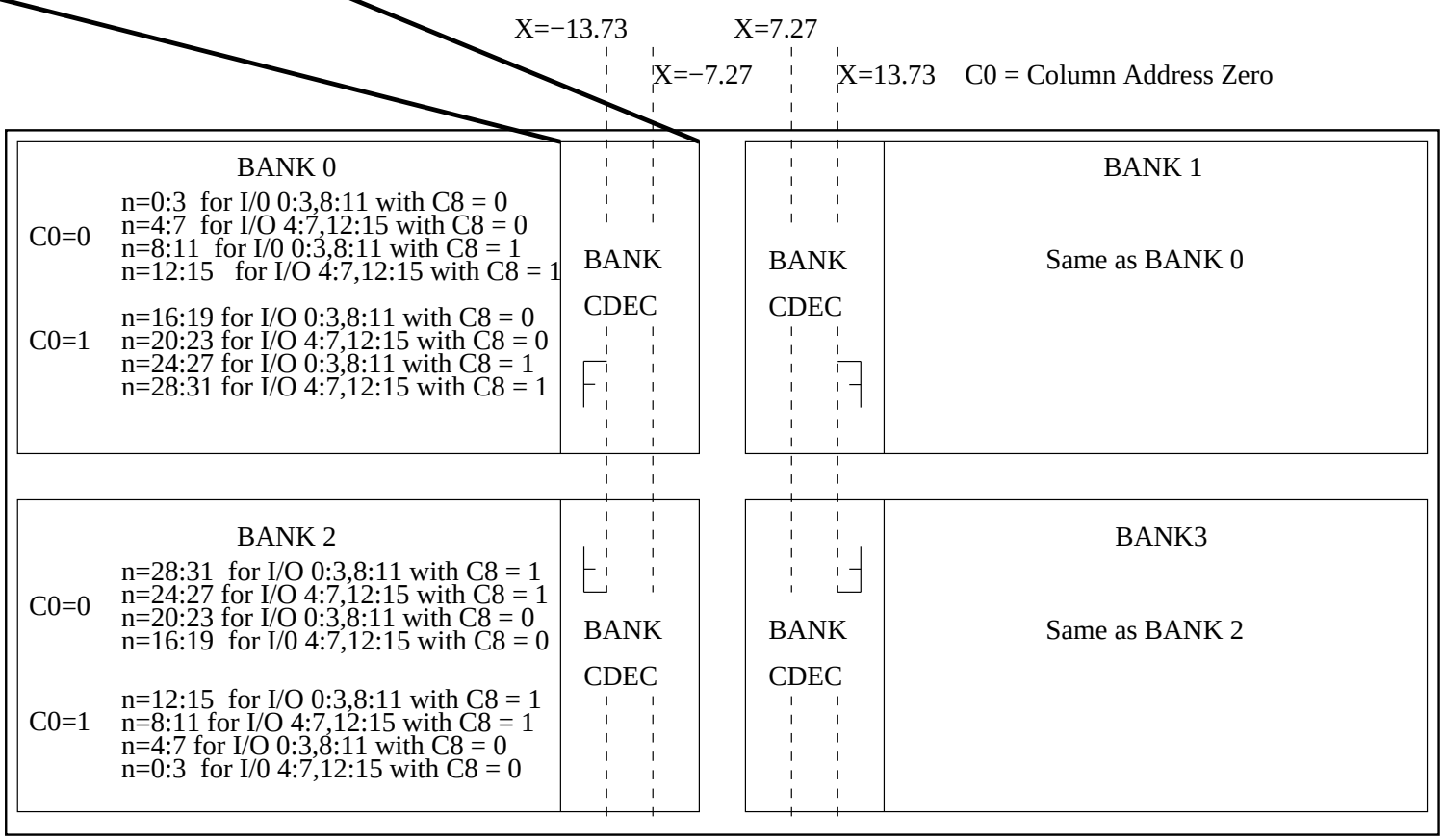


Bank 0,1 : Y(fx) = Y − n(75.68)

Bank 2,3 : Y(fx) = −Y + n(75.68)

n = Spare Column decoder number

Note: For banks 2 and 3, BANK CDEC is flipped vertically from banks 0 and 1.



colfusloc.fig

The following description refers to the QFUSE schematic and the COLUMN DECODER FUSE LOCATIONS document.

The column redundancy for the 128D14 consists of 32 spare column decoders per bank, with the chip containing a total of 4 banks. Each bank has 8 quadrants labeled CHLF. Each CHLF contains 4 spare column decoders. Each spare column decoder contains a total of 16 fuses which results in a total of 512 fuses per bank.

** Note: Of the 512 fuses/bank, only half are now used. The fuses corresponding to R11B on the QFUSE schematic are the only fuses used.

The schematic QFUSE contains 64 fuses representing the 4 spare column decoders in CHLF. The fuses are labeled RF(n)X where n is the spare decoder number (0:3) and X is the fuse number (0:15). Therefore, the notation RF23 refers to fuse 3 in spare cdec 2 and RF311 refers to fuse 11 in spare cdec 3. A description of the fuses is as follows:

Fuses RF(n)0 and RF(n)1 (which will now be referred to as F0 and F1) are enable fuses which are used to enable the selected spare column decoder.
Fuses F2 and F3 allow for programming with column address 1 (C1). Fuses F4 thru F7 allow for programming with the predecoded results of column addresses 3 and 2 (C32). Fuses F8 thru F11 allow for programming with the predecoded results of column addresses 5 and 4 (C54). Finally, fuses F12 thru F15 allow for programming with the predecoded results of column addresses 7 and 6 C(76).

The schematic QFUSE maps the above mentioned pairs of fuses to generic fuse numbers FC1 thru FC7. Fuse-blow tables have been created based on these generic fuse numbers which allow the required address to be programmed. The default address contained in the tables is a result of blowing only the enable fuse and no others for a given predecoded combination(i.e. FC4=NB and FC5=NB, C54<0> is chosen which is the default). Note that there are 4 separate fuse blow tables for C32<0>, C32<1>, C32<2> and C32<3>. This was done in order to create unique default addresses for the 4 spare column decoders within a CHLF. This allows for prefuse testing of the 4 spare columns and their decoders.

The 4 spare column decoders within a CHLF can be used to repair any column in that CHLF. There are specific requirements for determining which CHLF should be used for an observed failure on a given I/O. The following description will utilize the diagram 128D14 SPARE COLUMN DECODER FUSE LOCATIONS. For an observed I/O failure, the associated BANK number and the associated column address must be determined . With this information, the appropriate CHLF can be determined and a spare column decoder can be chosen. This is best demonstrated with an example:

Suppose BANK 0 is active.

```
                 C C C C C C C C C
                 8 7 6 5 4 3 2 1 0

Column Address = 0 1 0 1 1 0 1 1 1
```

I/O-8 is failing.

Step 1: Identify the bank and the state of C0 and the failing I/O,
and determine which spares are candidates for use.

For BANK 0, C0=0, C8=0, I0-8 ---> n=0:3

this indicates that spares 0,1,2 or 3 can be used.
(For this example, we will use 2)

Step 2: Refer to QFUSE sheet for programming.

Determine predecoded col addresses

C76=2 C54=3 C32=1 C1=1

Since spcdec<2> will be used,

Blow fuses RF20, RF22, RF24, RF26, RF28, RF210, RF214

Step 3: Determine fuse locations. Refer to Fuse locations sheet.

Since the above fuses are of the form RFnX, drop the n index and the leading R. This yields F0, F2, F4, F6, F8, F10, F14. Use the fuse number to determine the Y offset and use the equation for Y(fx) for Bank 0.

```
Y(F2)=  2866.73   - 2(75.68) , X= -7
Y(F0)=  2863.29   - 2(75.68) , X= -7
Y(F4)=  2859.85   - 2(75.68) , X= -7
Y(F6)=  2854.25   - 2(75.68) , X= -7
Y(F8)=  2832.33   - 2(75.68) , X= -7
Y(F10)= 2828.89   - 2(75.68) , X= -7
Y(F14)= 2819.85   - 2(75.68) , X= -7
```

I – POWER SUPPLIES

The attached table shows the target values for each mode of operation.

Voltages: Normal and Burn-in 01/02/02

	Normal Operation	DC Wafer Burn-in	AC Wafer Burn-in	Package Burn-in
VCCX	2.50 V	3.10 V	2.80 V	2.80 V
VINT	2.00 V	[VCCX]	[VCCX]	[VCCX]
VPP	2.90 V *(1.81*VBLH)*	4.49 V	4.06 V	[4.06 V]
VPL	0.80 V	1.60 V	1.40 V	1.12 V
VBLH	1.60 V	[2.48 V] *(0.80*VCCX)*	[VCCX]	[2.24 V] *(0.80*VCCX)*
VNWLL	-0.30 V	0.00 V	-0.30 V	-0.30 V
VBLEQ	0.80 V	0.00 V	1.40 V	1.12 V
VBB	-0.30 V	0.00 V	0.00 V	0.00 V

Note: For burn-in cases all voltages are forced (except those in brackets, which are internally generated.)

J- SPICE / EPIC METHODS

Both SPICE and EPIC used for verification.

The attached sheets describe the methods and types of simulations that were run.
A diagram of the full chip spice architecture is also included.

Main simulation directory: /ursa/jon/d14sp
D14.ckt primary .ckt file for SPICE and EPIC (sample is attached)
/ursa/jon/d14sp/timing contains all timing and .pat files
/ursa/jon/d14sp/epic contains all EPIC type files.
Typical run times for full chip SPICE to 100ns (~45minutes on Klondike)
Typical run times for EPIC to 100ns (~4 minutes)

The full chip simulation (Z14FULL) is set up as follows:
1 bank (#0)
2 wordlines, (WL0 is a redundant)
2 Y-addresses, (Y2 is a redundant)
Each Y address connects to even and odd data.
2 SABANDS, 1 slow side, 1 fast side
Each SABAND has 4 bits, 2 even and 2 odd.
A total of 4 DQs can be read in X16 mode, 2 in X4 mode.
(X4 and X8 mode are essentially the same for this simulation.)
The full control block (CONBLK) is included to verify function.
RABLK (row address block) and DPATH (data path) are placed as LVS versions to fully verify function.

K – MODELS

All nominal models were based on the 256MS14_TepsV0.3_2000DEC models.
Copies are attached here.

Best and worst case models were also developed.
These corner models were not based on actual silicon or results.
Doug did include an explanation of how each corner model was derived.

L – FILTER CAPS (DESCRIPTION AND VALUES)

All of the filter capacitors were built using the trench capacitor.
The attached ORCAD sheet shows how they were connected for each case.
The values obtained are also illustrated along with the sub-blocks they are located in.

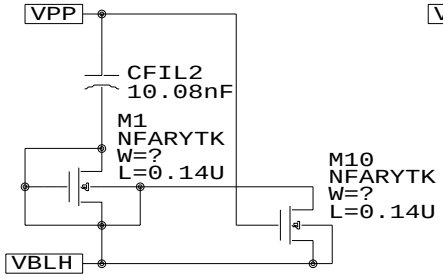
Values for LVS:

1 Trench is typically ~30fF.

In order to LVS, some special considerations were necessary.
The FCAP layer is used to merge the intermediate nodes of the filter cap structure into a common node, these makes it easier to run lvs. The structures in the attached sheet illustrate this.

A special transistor is also used for the filter caps, NF.
This device is created from a sub-set of the existing implants.

-The Nvt adjust is eliminated, this helps keep the NF's Vt lower.
-It does receive the VA implant, unfortunately this raises the Vt, but it can't be avoided since the filter caps are constructed over the buried well (cell array structure).

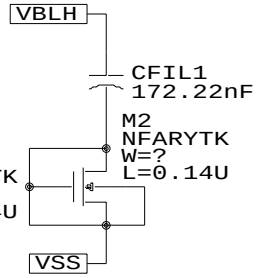


VPP - VBLH

BNKBOT = 10.08nF

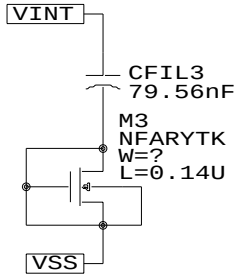
OF INSTANCES

BNKBOT (4X)
CHLF (32X)
COL (2X)
CONMISC (1X)
CPRDEC (4X)
D14PER (1X)
EDGE (4X)
LMISC (1X)
DCON (1X)
DLL (1X)
DPATH (1X)
DQSBLK (2X)
IOBLK (1X)
QBLK (16X)
RMISC (1X)
ROW1K (32X)
VINTTRM (1X)
VREF (1X)
VBG26 (1X)



VBLH - VSS

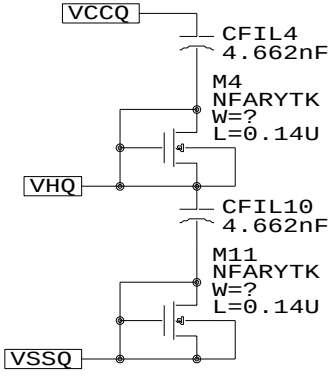
BNKBOT = 1.252nF
CHLF = 13.344nF
COL = 2.76nF
CONMISC = 40.69nF
CPRDEC = 1.120nF
D14PER = 39.7nF
EDGE = 59.2nF
LMISC = 14.15nF



VINT - VSS

BNKBOT = 1.608nF
CHLF = 18.91nF
CONMISC = 13.61nF
DCON = 1.07nF
DLL = .845nF
DPATH = 1.76nF
DQSBLK = .216nF
EDGE = 5.2nF
IOBLK = 17.52nF
LMISC = 12.31nF
QBLK = 1.024nF
RMISC = 4.85nF
ROW1K = .640nF

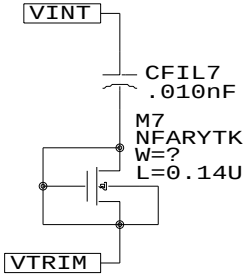
VCCQ - VHQ



DQSBLK = .518nF
QBLK = 4.144nF

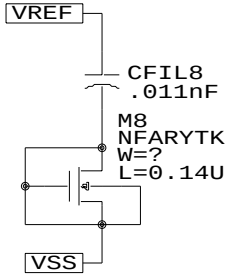
DQSBLK = .518nF
QBLK = 4.144nF

VHQ - VSSQ



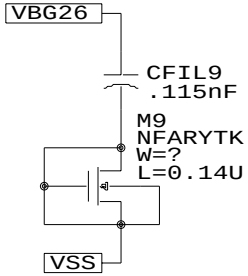
VINT - VTRIM

VINTTRM = .010nF



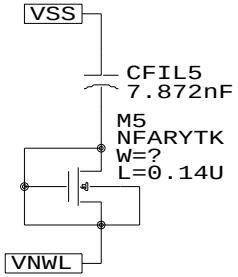
VREF - VSS

VREF = .011nF



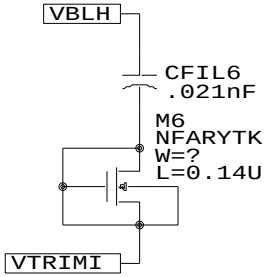
VREFBG - VSS

VBG26 = .115nF



VSS - VNWL

ROW1K = 7.872nF



VBLH - VTRIMI

VBLHTRM = .021nF

THIS SCHEMATIC IS A REPRESENTATION OF ALL
THE FILTER CAP ON THE CHIP. NOT A REAL SCHEMATIC.

UNITED MEMORIES INC. PROJECT: 128D14		
Title FCAP - FOR DOCUMENTATION ONLY		
Size A	Document Number FCAP	REV A
Date: December 27, 2001	Sheet 1 of 1	

M - ESD / LATCHUP

A copy of all ESD related schematics is included here for reference.

N – CURRENT DENSITY

The current density guidelines are attached.

C0 and C1 density checks are covered in the 128D14DRC_C0CHK and 128D14DRC_C1CHK rule set.

The M1 and M2 widths for maximum current density are not checked by CAD tools. They are derived and checked manually. This of course means the probability of error is high.

UMi United Memories, Inc

ALL01

Date: February 20, 2001

To: UMI

From: Doug Butler

Subject: S14 ELECTROMIGRATION

UMI has recently received from Infineon their S14 electromigration reliability rules (see attached). These rules do not allow for dimensional variation in the style of previous documentation. These rules also do not follow the method for calculating allowed AC current of previous methods. Nevertheless, we plan to follow the rules as listed.

UMI METHODOLOGY

1. We will assume that a 60/30 P/N transistor will be used to drive a 1pF load. This loading is heavier than the Infineon's assumption of a fanout of 3 but is closer to our typical design approach.

2. We will design with future parts in mind so the maximum frequency we will plan for is 250MHz. The first design will probably only run at 133MHz if it is a 128DDR replacement. All circuits will be checked with software to 125MHz and the designer is responsible to verify that the 250MHz sections of the circuit (a very small fraction of the layout) are OK for 250MHz. The reason for this is to minimize the impact of the electromigration rules on those parts of the circuits that are not running at 250MHz. Infineon provided UMI a table of only 167MHz data and I interpret from that they are designing only to 167MHz. I do not know what they are actually checking with software.

NEW RULES

The S14 rules contain AC current contact information. We have not had any rules for AC current in contacts up to now. The AC rules are based on RMS current (the amount of heating caused by the current). It appears that Infineon selected a 7X higher value for RMS contact current than DC current.

PLEASE NOTE THAT THE AC CASE IS NOW A CONCERN FOR NUMBER OF CONTACTS.

Please let me know if you do not agree with this approach or if the attached tables cause significant problems for layout.

ADDITIONAL CHART

I have added a summary sheet. The lines with the arrows are the only lines needed to determine the "standard" layout electromigration rules.

Doug Butler

4815 LIST DRIVE, SUITE 109 TEL (719) 594-4238
COLORADO SPRINGS, CO 80919 FAX (719) 594-4939

ELECTROMIGRATION RULES SUMMARY

60/30 P/N drives a 1pF load, 2.0V Vcc, Fast Models, 85C

Metal Layer	Thickness	Idc Max/uM^2	Iac Max/uM^2	Idc Max/uM width	Iac Max/uM width
	uM	mA	mA	mA	mA
M1	0.41	1.50	25.00	0.62	10.25
M2	1.10	1.60	15.00	1.10	16.50

Contact	Diameter	Idc Max/uM^2	Iac Max/uM^2	Idc Max/Contact	Iac Max/Contact
	uM	mA	mA	mA	mA
C1	0.18	1.00	7.00	0.025	0.178
C2	0.36	1.00	7.00	0.102	0.712

Contacts assumed to be round

DC (UNI-DIRECTIONAL CURRENT) LIMITS					
Frequency	Idc/u NMOS	C1s required	M1 width per	C2s required	M2 width per
	mA	per uM NMOS	uM NMOS	per uM NMOS	uM NMOS
20MHz	0.0013	0.05242	0.00217	0.01311	0.00121
125MHz	0.0083	0.32765	0.01355	0.08191	0.00758
250MHz	0.0167	0.65529	0.02710	0.16382	0.01515

AC (BI-DIRECTIONAL CURRENT) LIMITS					
Frequency	Iac/u NMOS	C1s required	M1 width per	C2s required	M2 width per
	mA	per uM NMOS	uM NMOS	per uM NMOS	uM NMOS
20MHz	0.0206	0.11589	0.00201	0.02897	0.00125
125MHz	0.0517	0.29020	0.00504	0.07255	0.00313
250MHz	0.0723	0.40628	0.00706	0.10157	0.00438

O – PARASITICS / OFF CURRENT / misc. PROCESS ISSUES

Parasitics: Resistance values were calculated by hand based on the final layout.
A look up table of commonly used sheet resistance values is attached here.

Capacitance values were extracted via software. A copy of the program is attached.
A table of commonly used dielectric thicknesses is also attached.

Off Current: Only minor considerations were taken to reduce off-current.

a) No NL (low Vt) devices were used outside the sense-amp in off situations. (They may be used somewhere as a permanent on transfer device.)

b) For any p-channel with its source at VCCP, an extra 0.1um was added to the gate length.

Misc. Process Issues:

None at this time.

P – LAYOUT

The top level cell name is “d14chip”.
The 0,0 origin is in the center.

From an assembly point of view, the chip was divided into 9 major sections.
BANK
COL
CONBLK
LMISC
DPATH
DCON
IOBLK
RABLK
RMISC

Each section can be DRCed and LVSed separately. See Section B- Architecture, for a more complete description.

A listing of the drawing layers and the mask gen table used is attached (layer table).

A complete listing of all the final checks run on the chip is attached (but not the results).

Run sets were written using both Calibre(Mentor) and Diva (Cadence) tools.

128d14 LAYOUT VERIFICATION(Recipe) CHECKLIST 01/29/2002
(Tape Ship Notebook Section 1.6.1)
Top cell for fracture: d14chip

VERIFICATION SECTION:

TOOL/ mode	TABLE/ cellname	CELL DELETION OPTIONS	RUNDATE	RUNTIME	STATUS	FILE SIZE
[CALIBRE]	DRC (DRC MAXIMUM RESULTS=100000)					
(hier)	d14chip	no option	01/28/02	2.3 hrs	Done	19meg
[CALIBRE]	DRC_005GRID (Checks all layers)					
(hier)	d14chip	no option	01/28/02	2 min	Done	empty
[CALIBRE]	DRC_010GRID (Checks all layers except DT)(rdary, 4megaryblt excluded)					
(hier)	d14per	no option	01/28/02	2 min	Done	empty
(hier)	col	no option	01/28/02	2 min	Done	empty
(hier)	saband_hm	option E	01/28/02	2 min	Done	empty
(hier)	bnkbot	option D	01/28/02	2 min	Done	empty
(hier)	chip_perim	no option	01/28/02	2 min	Done	empty
[CALIBRE]	DRC_ANTENNA (Ignore unattached power/signal runtime warnings)					
(hier)	d14chip	no option	01/28/02	8 min	Done	820
[CALIBRE]	DRC_C0CHK (Ignore unattached power/signal runtime warnings) (This check is for optimal layout construction. Not intended for onp/ary layout)					
(hier)	d14chip	no option	01/28/02	5 min	Done	182k
[CALIBRE]	DRC_C1CHK (Ignore unattached power/signal runtime warnings)					
(hier)	d14chip	no option	01/28/02	5 min	Done	250k
[CALIBRE]	DRC_C2CHK (Ignore unattached power/signal runtime warnings)					
(hier)	d14chip	no option	01/28/02	5 min	Done	21k
[CALIBRE]	DRC_C2G (DRC MAXIMUM RESULTS=40000) (This check is for optimal layout construction. Not intended for onp/ary layout)					
(hier)	d14chip	no option	01/28/02	5 min	Done	2.3meg
[CALIBRE]	DRC_DEN (Must leave memcell array in place)					
(hier)	d14chip	no option	01/19/02	20 hrs	Done	3k
[CALIBRE]	DRC_ERC (Ignore unattached power/signal runtime warnings)					
(hier)	d14chip	option A	01/29/02	11 min	Done	3k
[CALIBRE]	DRC_ERC_FWD_DIODE					
(hier)	d14chip	option A	01/28/02	15 min	Done	6.2k
[CALIBRE]	DRC_FIB_CHK					
(hier)	d14chip	option A	01/28/02	5 min	Done	empty
[CALIBRE]	DRC_FLTCHK					
(hier)	d14chip	option A	01/28/02	30 min	Done	55k
[CALIBRE]	DRC_PAD					
(hier)	d14chip	option A	01/28/02	5 min	Done	120k

```
--------------------------------------------------------------------------------
[CALIBRE]  DRC_POSTGEN
(hier)     d14chip       no option        01/28/02  15 min  Done    4.2k
--------------------------------------------------------------------------------
[CALIBRE]  DRC_PWRGRD (choose gdsii output type)(One run for each power supply)
(optional) d14chip       option A         11/20/01 5 min each Done
   POWER SUPPLY NAMES: vpp, vccx, vccq, vint, vblh, vss, vssq, vbb, vnwl
--------------------------------------------------------------------------------
[CALIBRE]  LVS (FINAL LVS ONLY) (d14chip includes WL's, BL's w/o memory AABIAS)
(hier)     d14chip       option A,C       01/28/02   3 hrs  Done    empty
(optional) bnkbot(w/WL's)  no option      01/28/02   5 min  Done    empty
(optional) hqsa_lvs(w/BL's)no option      01/29/02   5 min  Done    4 ports
(optional) col(w/ YL,FL's) no option      01/28/02   5 min  Done    empty
Note: Check pci_all, logo_revblk and sealring for correctness. The logo_revblk,
     pci_all and sealring cells create lvs errors. They are excluded from this run.
     Check the memcell aabias for interaction problems, since it's deleted in LVS.
LVS VALUES: RPT=BCDFS MP/MN/M(JN)/ME-W/L=1% SFT-W/L=1% C=1% R=1% DE=1% QP=1% WEFF=0
LVS FILTER-UNUSED: MOS=NO BIPOLAR=NO CAP=YES DIODES=NO RESISTORS=YES
LVS REDUCE: PARALLEL-MOS=YES PARALLEL-BIPOLAR=YES SPLIT-GATES=NO   SERIES-CAP=YES
            PARALLEL-CAP=YES PARALLEL-DIODES=YES  PARALLEL-RES=YES SERIES-RES=YES
LVS OPTION: IGNORE-PORT=YES RECOGNIZE-GATE=NO CAP-PIN-SWAPPABLE=YES VIRT-WIRE=YES
LVS FLAG: ACUTE NONSIMPLE OFFGRID SKEW                TEXT: USE TOP LEVEL TEXT ONLY
--------------------------------------------------------------------------------
[CALIBRE]  LVS_NOFC (FCAPS SMASHED)(d14chip includes WL's, BL's w/o memcell AABIAS)
(alternate)d14chip         option A,B     12/15/01  20 min  Done    empty
--------------------------------------------------------------------------------
EXCLUDED CELLS: (Alternate choice for option C, use option B for a 20 minute LVS run)
  option A = logo_revblk, pci_all,  sealring
  option B = 4m_arycelblt
  option C = memaabias, mem_core_edge, mem_core_l2, mem_core_l3, mem_core_l4,
             mem_core_l5, mem_core_b1, mem_core_b2, mem_core_b3, mem_core_m1,
             mem_core_m2, mem_core_m3, mem_core_t1, mem_core_r1, mem_core_r2,
             mem_core_r3, mem_core_r4
  option D = rdary, rdary_fill, rdary_av
  option E = sfet
(optional) = VERIFICATION OF THESE CELLS NOT REQUIRED DURING REVISIONS, OR TO
  FULLY VERIFY THE CHIP. SUB-CELLS MAY AID IN RE-VERIFYING THE LOCAL AREA BEFORE
  RUNNING FULL CHIP VERIFICATION. THEY ALSO MAY BE USED TO VERIFY INTERFACES.
  ALL VERIFICATION MUST BE RERUN EXCEPT FOR (optional), LAYER-GENERATION AND EXTRACT.
(hier) = Cell run in hierarchic mode, which is usually faster and simpler to debug.
LEGEND FOR DRC REPORTS: s = sign off(error plots required), f = false error(Explain),
  g = goes away next level up, e = edge error at array border or delcel edge.
--------------------------------------------------------------------------------
LAYER GENERATION SECTION: (Only needed for 1st release)
  XN & XP layers were drawn all through the project so generation is not needed.
  [SKILL]    CREATE GATEFILL/ (gate fill & fill hole layer generation)
    (flat)     (use SKILL "modify shapes", "generate fill" "follow steps 1-4") Done
  [SKILL]    CREATE AV/ (av implant layer generation)
    (flat)     (use SKILL "modify shapes", "generate fill","follow steps 7-8") Done
--------------------------------------------------------------------------------
```

```
-------------------------------------------------------------------------------
CAPACITANCE EXTRACT SECTION: (Only needed for 1st release)
  [DIVA]     PARAEXT/ (All run info is stored inside of doc/para_rpts)
  (flat)     bnkbot_para                    11/08/01  15 min  DONE
  (flat)     col                            10/16/01  15 min  DONE
  (flat)     conblk                         11/21/01  15 min  DONE
  (flat)     dcon                           10/16/01  15 min  DONE
  (flat)     dll                            12/07/01  15 min  DONE
  (flat)     dpath                          10/16/01  15 min  DONE
  (flat)     eclk                           12/04/01  15 min  DONE
  (flat)     fdel                           12/07/01  15 min  DONE
  (flat)     hqsa                           12/07/01  15 min  DONE
  (flat)     ioblk                          10/15/01  15 min  DONE
  (flat)     left                           10/17/01  15 min  DONE
  (flat)     rab_wire_para                  11/08/01  15 min  DONE
  (flat)     row1k_para                     11/08/01  15 min  DONE
  (flat)     vdel                           12/04/01  15 min  DONE
  (flat)     vnosc                           7/10/01  15 min  DONE
  Extra balancing was done on COL DAMP and DLL regions using net to net extracts.
-------------------------------------------------------------------------------
  SILICON IMAGER:
    Use /saturn/larry/cds/128d14/doc/umi_s14a.model for simulation model.
    To create model, run /cad/cadence/assura/tools/assura/bin/simodgen using
      /saturn/larry/cds/128d14/doc/umi_s14a.par for model generation.
    See /melinda/kenj/pdf/simod.pdf for Simodgen manual.
    See /melinda/kenj/pdf/silimage.pdf for Silicon Imager manual.
    See /melinda/kenj/pdf/sical.pdf for Simodcal manual.
    Limitations: All active's must merge to one layer to run Silicon Imager.
    Use 0.001 grid while running imager to reduce contour line shift caused by
      grid snapping.
    Layer setup was created using one third width and one third space conditions,
      which is the worst case exposure ranges.
    For Trench layer: (DT) Choose Dark Field(CN) and set contour
      levels to two: (Low=0.215, High=0.44)
    For Active layers: (ND,PD,AABIAS) Choose Bright Field(CP) and set contour
      levels to two: (Low=0.208, High=0.38)
    For Poly layers: (GC,GCS) Choose Bright Field(CP) and set contour
      levels to two: (Low=0.195, High=0.395)
    For M0 layers: (M0,M0a) Choose Dark Field(CN) and set contour
      levels to two: (Low=0.195, High=0.395)
    For M1 layers: (M1,M1a) Choose Bright Field(CP) and set contour
      levels to two: (Low=0.195, High=0.395)
-------------------------------------------------------------------------------
MISCELLANEOUS INFORMATION:
  The version of stream used keeps the rods/pcells/symbolics as cells for a quicker
    stream out and smaller stream file size. Do not stream out and back into the
    database, since pcells parameters will be lost. There are extra cells in the opus
    database that are not contained in the chip hierarchy(LVS cells, pcells etc...)
  The power c2's were used extensively on this chip.
    These power c2's have a 4-8um rectangle shape.
  A hand check has been done on the delcel'ed regions: logo_revblk,pci_all,sealring
    cells looking for any intruding polygons.
  ACCEPTABLE STREAM WARNINGS: (NONE)
  The netlist in d14chip run was modified to delete the vpl port which use to be
    a pad connection, however it has since been removed but the schematic was
    never updated.
  The hqsa_lvs cell was not built to run hierarchically and there are 4 ports that
    it complains about since they are not I/O ports in the schematic. OK as is.
-------------------------------------------------------------------------------
```

S14 LAYERS USED FOR MASK MAKING:				January 17, 2002
Layer Name	**Purpose**	**Layer**	**D-type**	**Layer Description**
dt	drawing	4	0	Trench layer in memcell and fcap
wn	drawing	2	0	nwell layer
wb	drawing	1	0	deep nwell layer used to create isolated pwells
aabias	drawing	5	4	active layer used in memcell and fcap
aabias	serife1	5	61	shaping layer for aabias/cb contact used in memcell
av	drawing	6	0	CMP oxide removal layer for active
nd	drawing	5	5	Nchannel active layer for core and periphery
pd	drawing	5	6	Pchannel active layer for core and periphery
fh	drawing	39	0	fill hole active layer over gate fill only
xn	drawing	19	0	N+ implant layer
xp	drawing	20	0	P+ implant layer
va	drawing	9	0	implant used over memcell and fcap
vk	drawing	40	0	thick oxide gate layer
vl	drawing	12	0	lowVt implant for Nchannel transistors
vm	drawing	10	0	lowVt implant for Pchannel transistors
gc	drawing	16	0	poly layer used for periphery/core interconnect and gate regions
gcs	drawing	16	3	poly layer used for memcell/fcap interconnect and gate regions
gf	drawing	17	0	poly gate fill layer for planarization
cb	drawing	21	0	memcell and fcap S/D contact layer
c0	drawing	22	0	periphery and core S/D and poly contact layer
cf	drawing	38	0	poly contact for gate fill poly only
m0	drawing	24	0	periphery/core metal0 interconnect layer
m0	array	24	10	memcell/fcap metal0 interconnect layer
c1	drawing	25	0	metal0 to metal1 contact layer
m1	drawing	26	0	periphery/core metal1 interconnect layer
m1	array	26	10	memcell/fcap metal1 interconnect layer
c2	drawing	27	0	metal1 to metal2 contact layer
m2	drawing	28	0	metal2 interconnect layer
tv	drawing	29	0	pad and fuse window passivation opening layer
second	drawing	60	0	Used to cover both rings in seal ring
(aa drawing, aa core, nd core, pd core are not used)				
(vpd drawing not used since the depletion device is not supported)				
(cd drawing is renamed to c0 drawing and S/D and poly contacts exist on this layer)				
(cg drawing is not used since all poly contacts exist on c0 drawing)				
(gc core, m0 core, m1 core are not used since Infineon useage was not consistent)				
(tv drawing1 not used, htck (all purposes) not used, dt serife1 and serife2 not used)				
(aabias serife2 not used, all kerf layers not used, sn drawing not used)				
(cgf drawing is renamed to cf drawing and listed above)				
(gcfh drawing is renamed to fh drawing and listed above)				
S14 LAYERS USED BY VERIFICATION:				
Layer Name	**Purpose**	**Layer**	**D-type**	**Layer Description**
trim	drawing	53	1	In and Out wiring option resistors for checking circuit options
border	drawing	55	0	cell extent and cellname text for plotting
txt	drawing	0	0	device number and signal name text for plotting
gctxt	label	0	2	gc text label for port labeling in LVS
m0txt	label	1	2	m0 text label for port labeling in LVS
m1txt	label	2	2	m1 text label for port labeling in LVS
m2txt	label	3	2	m2 text label for port labeling in LVS

tvtxt	label	4	3	tv text label for port labeling in LVS
marker	error	N/A	N/A	DRC output layer for Calibre
drcout	drawing	50	0	DRC output layer for Dracula
ary	drawing	53	13	cover layer to identify the array region
sdef	drawing	53	16	cover layer to identify the sfet device in samp
fcap	drawing	53	12	cover layer to identify the fcap device
rdec	drawing	53	17	cover layer to identify the rdec special rules
resg	drawing	53	7	cover layer to identify the poly resistor
resj	drawing	53	9	cover layer to identify the jfet device
resn	drawing	53	6	cover layer to identify the N-diffusion resistor
resw	drawing	53	8	cover layer to identify the Nwell resistor
fuse	drawing	53	2	cover layer to identify the fuse device
bip	drawing	53	5	cover layer to identify the bipolar device in ESD
diode	drawing	53	10	cover layer to identify the diode device in ESD and under pad
rpad	drawing	53	18	cover layer to identify the multidie probe pad
gfblank	drawing	53	4	cover layer to exempt gate fill generation
gc	net	N/A	N/A	landing layer for DIVA parasitic extract saved interconnect layer
m0	net	N/A	N/A	landing layer for DIVA parasitic extract saved interconnect layer
m1	net	N/A	N/A	landing layer for DIVA parasitic extract saved interconnect layer
m2	net	N/A	N/A	landing layer for DIVA parasitic extract saved interconnect layer
tv	net	N/A	N/A	landing layer for DIVA parasitic extract saved interconnect layer

S14 MASK FRACTURE ALGORITHM				January 15, 2002	
Mask Layer	**Mask Polarity**	**GDS Layer Layer #;Dtype**	**Fracturing Algorithm**	**Sizing (um/side)**	**Shrink Factor**
DT	CN	DT(4;0)	DT		x1
AA	CP	ND(5;5)	(AABIAS + AABIAS_s1 +		x1
		PD(5;6)	ND + PD + FH)		
		AABIAS(5;4)			
		AABIAS_s1(5;61)			
		FH(39;0)			
AV	CN	AV(6;0)	AV		x1
WN	CN	WN(2;0)	WN		x1
VM	CN	VM(10;0)	VM		x1
WP	CP	WN(2;0)	WN		x1
VN	CP	WN(2;0)	(WN + VL + VA)		x1
		VL(12;0)			
		VA(9;0)			
WB	CN	WB(1;0)	WB		x1
VA	CN	VA(9;0)	VA		x1
VK	CP	VK(40;0)	VK		x1
GC	CP	GCS(16;3)	((GCS + GC + GF) - FH)		x1
		GC(16;0)			
		GF(17;0)			
		-FH(39;0)			
XN	CN	XN(19;0)	XN		x1
XP	CN	CP(20;0)	XP		x1
CB	CN	CB(21;0)	CB		x1
CS	CN	C0(22;0)	(C0 + CF)		x1
		CF(38;0)			
M0	CN	M0(24;0)	(M0 + M0_array)		x1
		M0_array(24;10)			
C1	CN	C1(25;0)	C1		x1
M1	CP	M1(26;0)	(M1 + M1_array)		x1
		M1_array(26;10)			
C2	CN	C2(27;0)	C2		x1
M2	CP	M2(28;0)	M2		x1
TV	CP	TV(29;0)	TV		x1
Note: Second Drawing(60;0) will be used in seal ring on mask layer CS, C1.					

Q – MASK / ALIGNMENT ETC.

We have no information pertaining to alignment.

R – MISCELLANEOUS DESIGN INFORMATION

Libraries used for Schematics:
/ram1/cad/pclib/s14.lib
/ram1/cad/pclib/s14log.lib

Some Design Guidlelines:

Flip-Flop Reset Ratios, at least 6:1 (n:n, equivalent) is the minimum.

Test mode signals all start with name “TM…..”

Any signal ending in “….b” is active low.

Signals ending in “..vcc” or “..vss” are DC and do not switch, and can route in anything.

S – RELATED DATA SHEETS

T- GENERAL INFORMATION (NOTES, MEMOS, ETC.)

Any information relevant to defining the chip may be included here.
Key memos or reports that define critical decisions, or data, would be an example of what might be found here.

```
------------------------- Archive Tape README File: --(Notebook section 1.7.0)--
### Sample README file for layout documentation ### Template Rev. Date: 08/06/96
    (INCLUDE A HARDCOPY OF THIS COMPLETED FILE WITH THE TAPE SHIP NOTEBOOK)
-------------------------------------------------------------------------------
FORMAL TAPE NAME(i.e.: Part#_Mo=01, Day=29, Year=02): 128d14_A0_012902
REVISON NAME: A0
 DO NOT USE REVISION A0_010402 or A0_012002 tape, no masks made from these tapes
TOP CELL NAME:                                  d14chip
DESIGN RULE DOCUMENT NAME & REVISION DATE:
 UMI S14 DESIGN DOCUMENT                REVISION r03
IS THIS ARCHIVE OK TO USE FOR FUTURE REVISIONS: yes
LAYOUT: Larry Aldrich, GW Jones, Penny Austin, Mark Bartlett, Carol Gruenschlaeger
DESIGN: Jon Faue, Brett Meadows, John Heightley, Craig Barnett, Van Butler
LAYOUT SOFTWARE/REVISION/HARDWARE: Opus LayoutPlus version 4.4.5/Sparc-Ultra
VERIFICATION SOFTWARE/REVISION/HARDWARE:
 Calibre v8.8_2.1    Mon Aug 21 23:13:47 PDT 2000 /
 SunOS valdez 5.6 Generic_105181-16 sun4u /Sparc-Ultra
CADENCE LAYERS MENU:                       display.drf, techfile.cds, techfile.source
CADENCE LAYERS STREAM CONVERSION TABLE:    techfile.cds
CADENCE TEXT FONT:                         (0) 3000 Stick, (1) 10000 roman, (2) 5000 Europe
STREAM OUT / STREAM IN SOFTWARE:           stream (in/out)
   STREAMOUT OPTIONS:
      Option: all boxes will appear as polygons in the STREAM file.
      Option: all pcells and symbolics will remain intact as unique $$ cells.
      Option: block names will be preserved as the same case.
      Option: remove co-incident and co-linear points for polygon, path and line.
      Option: all STREAM property attribute information will be ignored.
      Data base units will not be scaled.
   STREAMIN OPTIONS:
      Option: STREAM names will be converted to lower case.
      Option: STREAM arrays will be converted to mosaics.
      STREAM data base units will not be scaled.
STREAM FILE DBASE UNITS PER USER UNIT:  (1000), BASIC GRID:=0.001,      UNIT:=um
CADENCE DBASE UNITS PER USER UNIT:      (1000), BASIC GRID:=0.01,       UNIT:=um
VERIF. TABLES DBASE UNITS PER USER UNIT:(1000), BASIC GRID:=0.001/0.001,UNIT:=um
```

```
--------------------------------------------------------------------------------
CHIP HIERARCHY(major blocks only): d14chip,chip_half(2),d14per,pci_all(4)
--------------------------------------------------------------------------------
UNDOCUMENTED LAYERS NOT FOUND IN DESIGN RULES(i.e.: option mets, lvstxt etc.):
  STRM-LAY# TYPE  CADENCE-LAYERNAME-PURPOSE DESCRIPTION
  See techfile.source layers table. (Include hardcopy w/ tape ship notebook).
  See mask table and mask layers printouts or look in doc directory.
  No option layers used. Trim layer used to verify In/Out wiring options.
   0 datatype 0     txt-dg txt device#,signal names plotting text layer.
   0 datatype 2   gctxt-dg GC LVS text layer for verification.
   1 datatype 2   m0txt-dg M0 LVS text layer for verification.
   2 datatype 2   m1txt-dg M1 LVS text layer for verification.
   3 datatype 2   m2txt-dg M2 LVS text layer for verification.
   4 datatype 3   tvtxt-dg TV LVS text layer for verification. (Not used)
   5 datatype 61 aabias-s1 aabias shaping serifes used in memcell.
  16 datatype 3     gcs-dg gc poly layer for the memory cell.
  22 datatype 0      c0-dg c0 contact layer for active and poly. C0=(CD or CG)
  24 datatype 10     m0-ay m0 bitline layer for the memory cell.
  26 datatype 10     m1-ay m1 wordline layer for the memory cell.
  26 datatype 20     m1-bc m1 used in seal ring cell. (Promos addition)
  38 datatype 0      cf-dg gatefill poly contact layer. (CF=CGF)
  39 datatype 0      fh-dg fillhole active layer. (FH=GCFH)
  55 datatype 0   bordr-dg bordr cell extent and cellname plotting text layer.
  53 datatype 1    trim-dg trim recognition layer for In/Out wiring.
  53 datatype 2    fuse-dg fuse recognition layer for verification.(m1 fuse)
  53 datatype 4 gfblank-dg masks gate fill during gate fill generation.
  53 datatype 5     bip-dg bip bipolar vpnp device recognition layer.
  53 datatype 6    resn-dg resn ndiff resistor recognition layer.
  53 datatype 7    resg-dg resg poly1 resistor device recognition layer.
  53 datatype 8    resw-dg resw nwell resistor device recognition layer.
  53 datatype 9    resj-dg resj jfet device recognition layer.
  53 datatype 10  diode-dg diode esd diode device recognition layer.
  53 datatype 11    esd-dg esd recognition region for drc segregation.
  53 datatype 12   fcap-dg fcap recognition region for verification.
  53 datatype 13    ary-dg ary memcell recognition region for drc segregation.
  53 datatype 14    onp-dg onp saband,rdec,col recognition for drc segregation.
  53 datatype 15   samp-dg samp recognition region for drc segregation.
  53 datatype 16   sdef-dg sdef saband sfet device recognition layer.
  53 datatype 17   rdec-dg rdec recognition region for drc segregation.
  53 datatype 18   rpad-dg pads to be probed on multidie probing.
  60 datatype 0  second-dg layer used in seal ring. (Promos addition)
--------------------------------------------------------------------------------
****************    ARCHIVE TAPE DIRECTORY LISTING   ****************
  font, gds.lyr, layers/,layout/, workhdrc/, workhlvs/, schematic, spice,epic
  (rulescadence/, ruleshdrc/, ruleshlvs/, must be cad to load w/ readtape)
README LOCATION:                                        layout/doc/README
VERIFY_RECIPE LOCATION:                                 layout/doc/verify_recipe
PARASITIC CAP. FILES:                                   layout/doc/para_rpts/*
OTHER MISC. DOC FILES:                                  layout/doc/*
--------------------------------------------------------------------------------
COMMENTS:
  See plot_pcells s14_pcells library for pcells used in this chip.
```

```
--------------------------------------------------------------------------------
DOCUMENT LAYER GENERATION PROCEDURES:
  1) The gate fill and fill holes are generated in all the open regions outside of
     existing active and gate regions using the diva/skill routines.
  2) The av layer is generated inside of all active regions that are large enough
     to meet the minimum width rule, and have been added to fcap hiearchy too.
  3) The m1 minimum fill metal fingers have been added by hand to create m1 features
     at least every 11um.
--------------------------------------------------------------------------------
ACCEPTABLE STREAM OUT WARNINGS: None
--------------------------------------------------------------------------------
Chip size data extent with seal ring but without streets: 5768x5833um (1x)
--------------------------------------------------------------------------------
MISCELLANEOUS INFORMATION:
--------------------------------------------------------------------------------
LAYOUT DATA - Is included in opus format with pcells turned into unique instances.
      stream file: d14chip.gds
            d14chip - top level structure for verification and mask making.
--------------------------------------------------------------------------------
VERIFICATION DATA:
  verify_recipe - describes the required verification runs and excluded cells.
  d14chip.net - the netlist used for final lvs - top subcircuit is "chip".
A copy of the .rep file, short.rpt exists in each drc directory.
--------------------------------------------------------------------------------
pad_coords.xls - The pad coordinates based on chip with its center at 0,0.
fuse_coords - See tape ship notebook or Brett Meadows for document.
--------------------------------------------------------------------------------
```

128D14 Tape Ship December, 2001

The 128D14 Design is complete and ready for fracture in the 0.14um S17 process.

Along with the tape, there are 3 pieces of documentation that we completed.

1) A 128D14 Schematic Notebook:
   This shows all LVS and SPICE schematics for the chip.

2) A 128D14 Design Manual:
   This is a collection of notes and diagrams that explains as best we can how the chip is actually built. Repair instructions, scramble tables, and bonding diagrams are an example of what is found in this manual.

3) A 128D14 Tape Ship Book:
   The Tape Ship book contains proof of the LVS/DRC/ERC runs that were used in the final checking of the chip.

   This list will become more useful as revisions are needed.

All documentation in this book should be updated accordingly.

List of Infineon's Documentation:

Since the process and the starting database (256M S14 SDRAM) were obtained from Infineon, we relied heavily upon their documentation. The following is a list of all the Infineon documents we found relevant. Any information we didn't provide can probably be found there.

Title: Product Description
256M Product Description S14 DD1A
Date: 01/18/01
Version: .1.1

Title: 0.14um Design Manual for DRAM Products
Date: 11/08/01
Version: 3.0

Title: 0.14um Process Assumptions for DRAM Technology
Date: 11/08/01
Revision: 3.0

REVISION HISTORY

NOTE: The revision numbers on this .pdf document do not necessarily bear any relation to the revision numbers in the database.

DATE	REVISION	MODIFICATIONS
01/20/02	128D14_MAN_A0	Original document
02/07/02	128D14_MAN_1	Added Bit Line Twist diagrams to the Architecture section.